

University of Central Florida



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Adaptive Behavioral Simulation Framework for 2-Terminal MTJ-based Analog to Digital Converter

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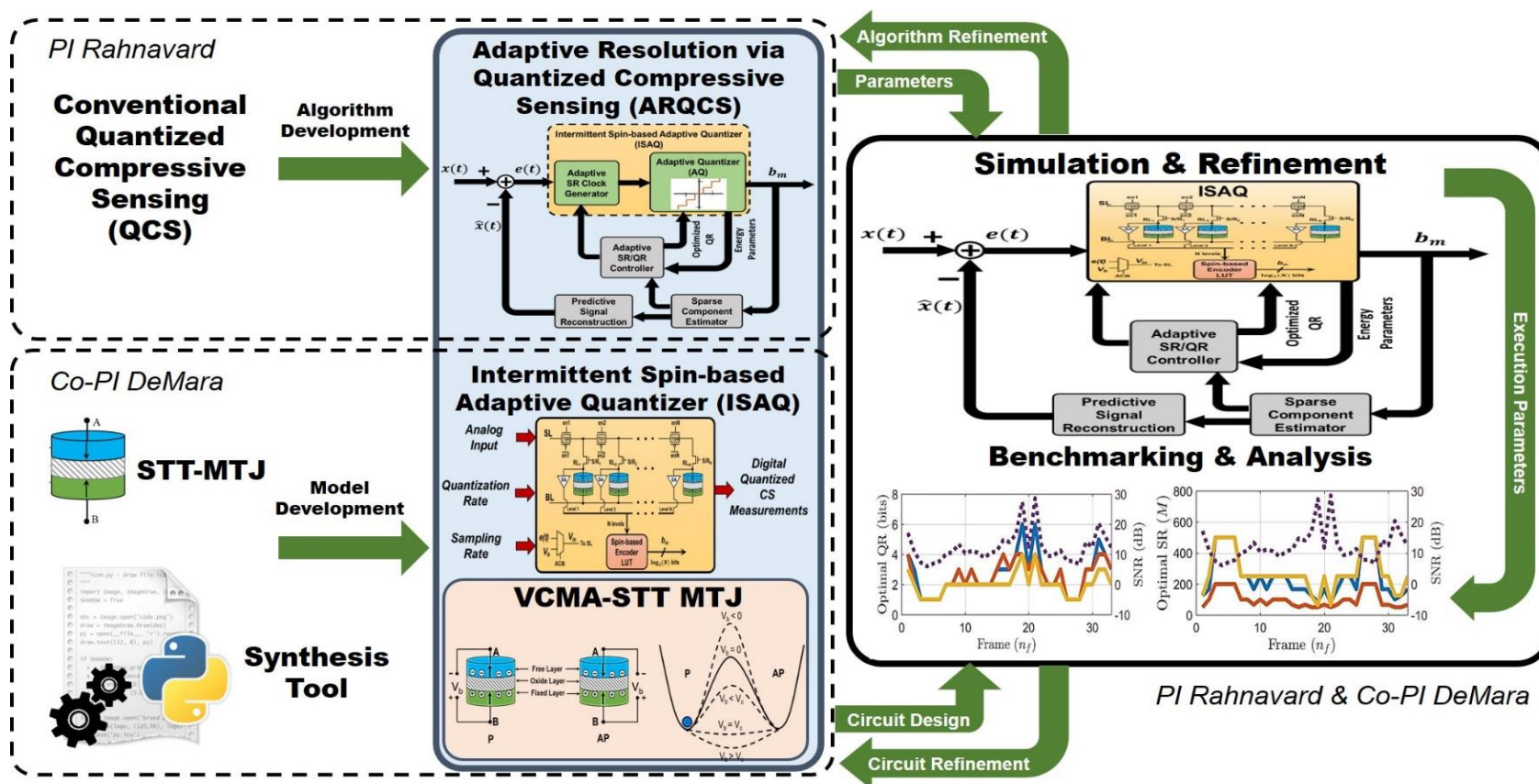
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Saturday, August 1, 2020 via Zoom meeting

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“Cross-layer Adaptive Rate/Resolution Design for Energy-Aware Acquisition of Spectrally Sparse Signals Leveraging Spin-based Devices”

- Develop energy-efficient adaptive framework to acquire spectrally-sparse signals
- Integrate adaptive quantized Compressive Sensing w/ beyond-CMOS devices





Three Pathways to Educational Impacts

Research Expertise ↔ REU Experiences ↔ High School Outreach

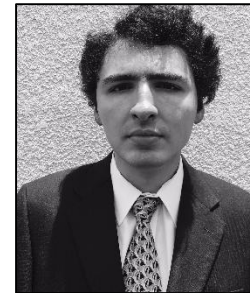
Spintronic
Educational
Simulation

1)
Foster
Scholarly
Research
Expertise

Doctoral Graduates / Students



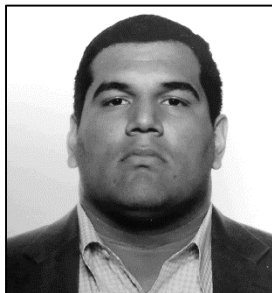
Soheil Salehi, Ph.D.
Completed Ph.D.; now a
Post-Doctoral Researcher
at UC-Davis



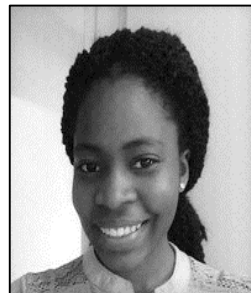
Adrian Tatulian, M.S.
Doctoral Student

2)
Mentor
Impactful
REU
Experiences

REU Graduates / Students



Gustavo Camero
Completed REU; now
a Doctoral Student at
Carnegie Mellon Univ.



Adedoyin Adepegba
REU currently
interning at Intel



Paul Wood
REU currently
interning at Intel



Daniel C. Mulvaney
REU currently
interning at L3-Harris



Three Pathways to Educational Impacts

Research Expertise ↔ REU Experiences ↔ High School Outreach

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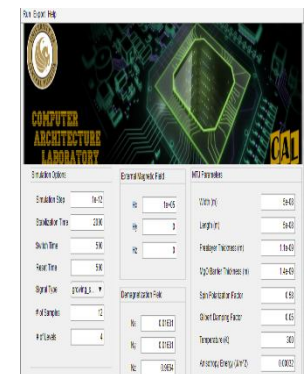
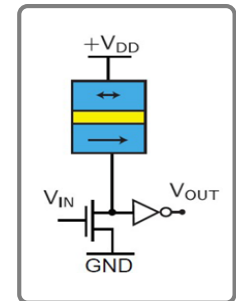
3) Creating Educational Outreach for High Schoolers

Outreach Goals & Approach

- **Mentor** U/G's via NSF REU supplement
- **Paid REUs** conducted lit surveys of signal encoding/conversion, performed SPICE simulations w/ MTJ circuits designed by GRAs
- **REUs learned** SPICE circuit modeling tools via structured examples, and practiced proofreading of articles composed by team members, post-CMOS technical knowledge and authoring skills

Spintronic Simulation Website

- **Simulation Framework** is an educational resource site companion to distribute the interactive tool to provide insights of the modeled Spin-based ADC
- **Broad dissemination** through web-based framework to maximize the impact of outreach

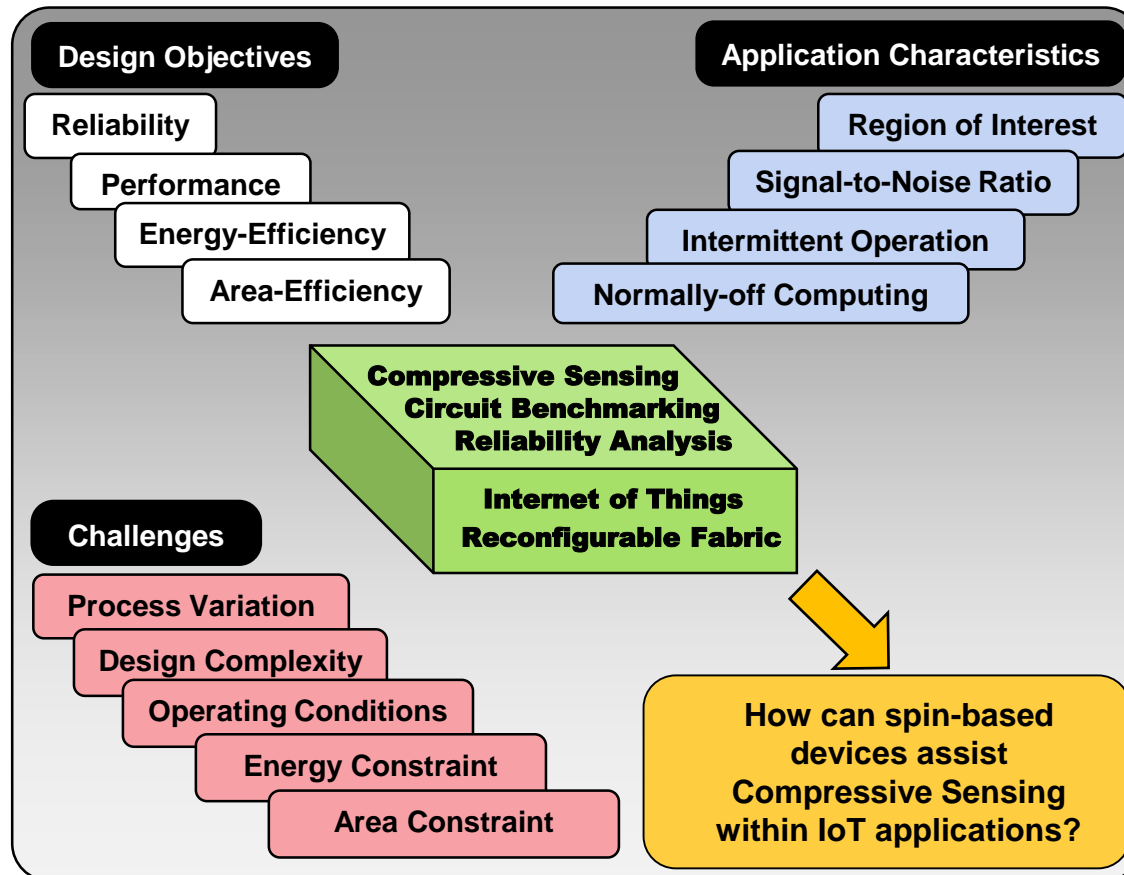




Research Motivation

Need for CS solutions considering device-level constraints for IoT

- ✓ There is a need for low-complexity, ultra-low-power circuit for signal conversion for IoT applications
- ✓ There is a demand for Compressive Sensing solutions that consider hardware constraints and signal constraints for IoT intelligent sampling and edge processing

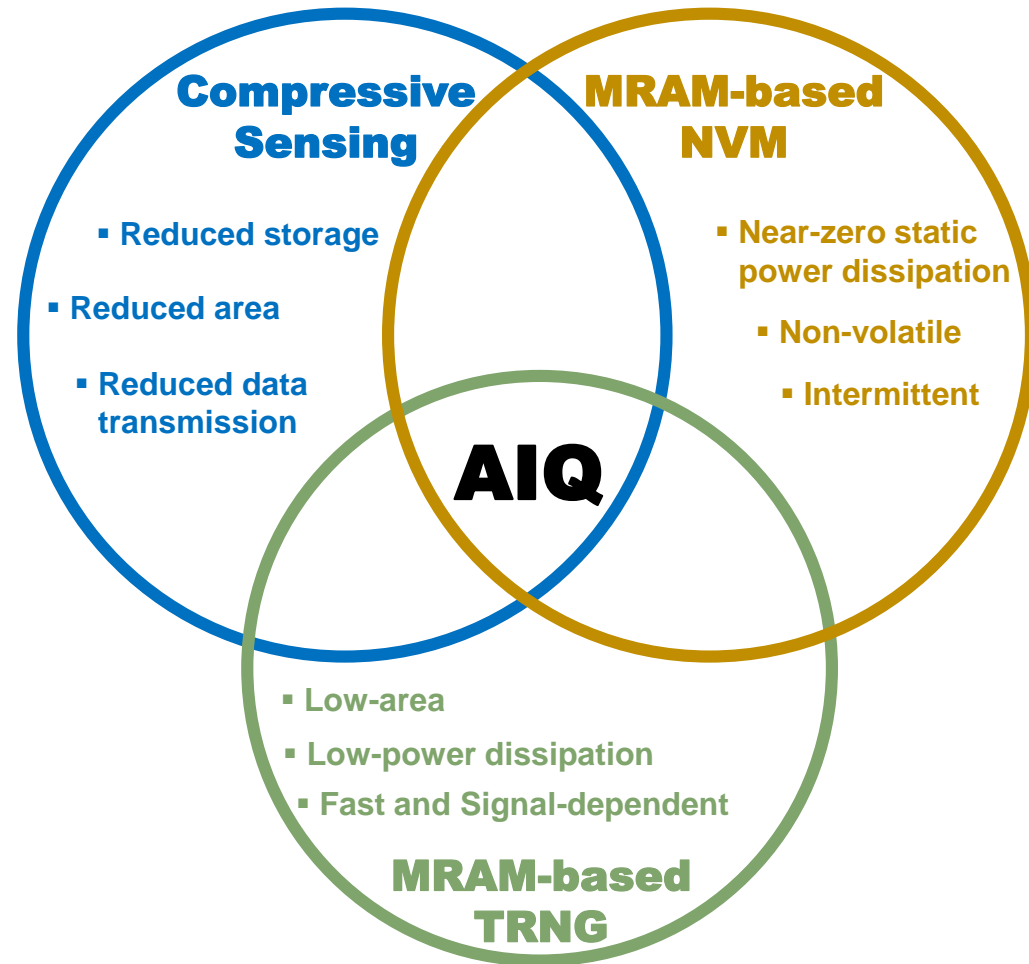




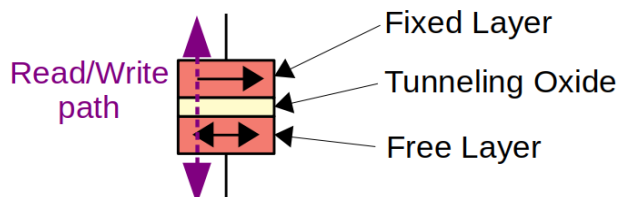
Research Motivation

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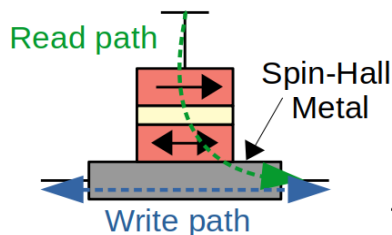
- Maximize signal sensing and reconstruction performance while **reducing energy consumption for IoT applications**
- **Compressive Sensing** reduces number of samples per frame to **decrease energy, storage, and data transmission overheads**
- Non-uniform CS in hardware requires Random Number Generator (RNG)
 - True RNGs vs. Pseudo RNGs



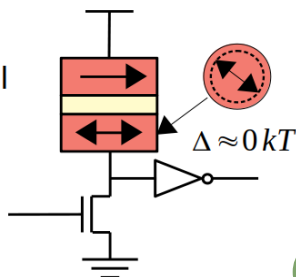
Magnetic Tunnel Junction



SHE-MTJ



Embedded p-bit



Advantages

- ✓ Near-zero standby power
- ✓ Area efficient
- ✓ Fast read operation
- ✓ True randomness

- **Magnetic tunnel junctions (MTJs)** consist of a tunneling oxide layer sandwiched between two ferromagnetic layers.
- Magnetization of free layer can be modified using a current or voltage.
- **Low-barrier MTJ** can be used to build Magnetic Random Access Memory (MRAM)-based **p-bit with stochastic switching capability**



Intel now delivering embedded MRAM (eMRAM) in a 1T1MTJ architecture in conjunction with their 22-nm FinFET technology libraries¹

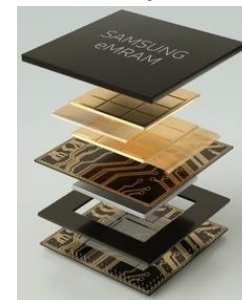


Everspin & IBM MTJ-based SSD and DRAM replacement products available



Toshiba is fabricating SHE-MTJ²

https://www.theregister.co.uk/2019/03/08/samsung_mram/



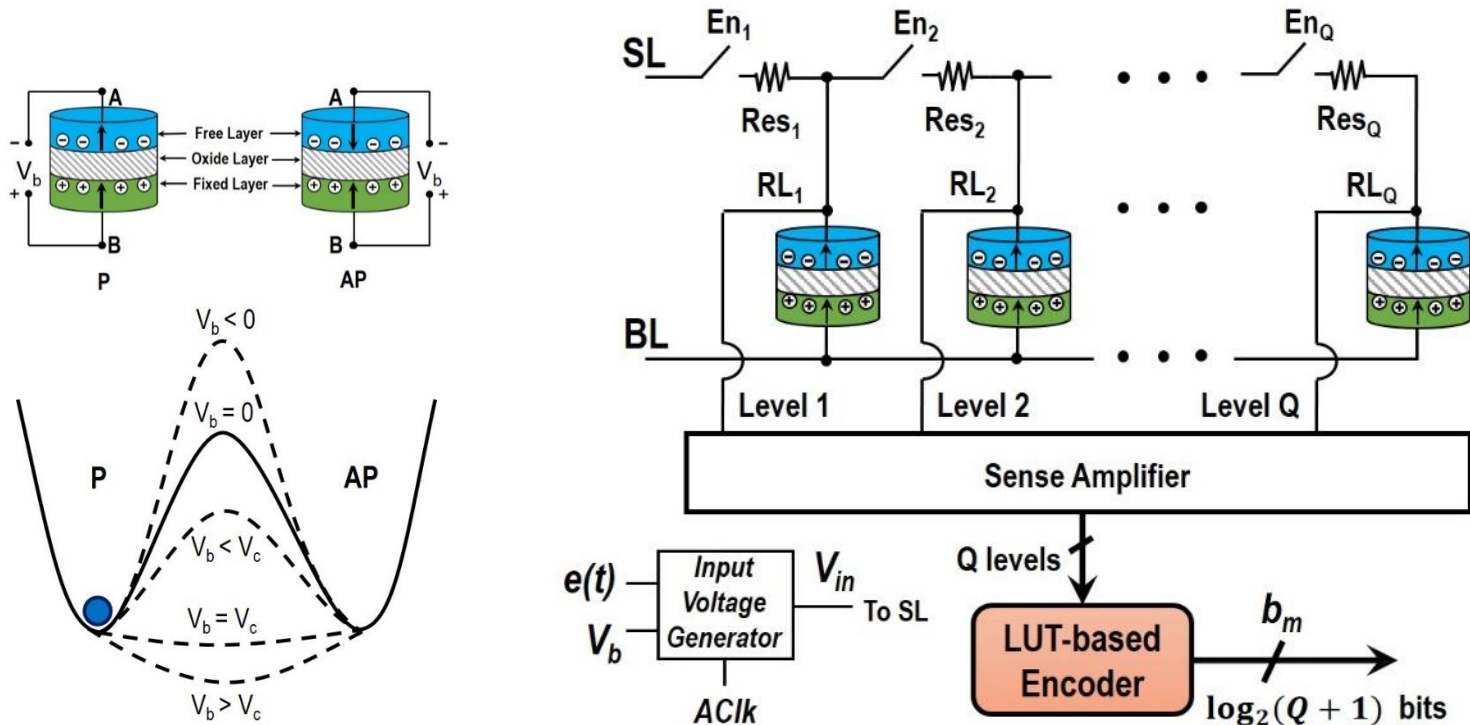
<https://www.everspin.com/spin-transfer-torque-mram-products>

1. Wei, Liqiong, Juan G. Alzate, Umut Arslan, et al. "13.3 A 7Mb STT-MRAM in 22FFL FinFET Technology with 4ns Read Sensing Time at 0.9 V Using Write-Verify-Write Scheme and Offset-Cancellation Sensing Technique." In *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 214-216, 2019.

2. H. Yoda et al., "High-Speed Voltage-Control Spintronics Memory (High-Speed VoCSM)," 2017 IEEE International Memory Workshop (IMW), Monterey, CA, 2017, pp. 1-4.

Voltage-Controlled Magnetic Anisotropy Magnetic Tunnel Junction (VCMA-MTJ) AIQ

- 1) **During Reset step:** all active VCMA-MTJs are reset to Parallel state
- 2) **During Sampling step:** based on determined SR and QR, first bias voltage, V_b , is applied across the active VCMA-MTJs to modify energy barrier followed by analog input, $e(t)$, to write into the active VCMA-MTJs
- 3) **During Read step:** use a sense amplifier to read data stored in each VCMA-MTJ



1. S. Salehi, M. Mashhadi, A. Zaeemzadeh, N. Rahnavard, and R. F. DeMara, IEEE JETCAS-2018

2. This work is funded by NSF-ECCS #1810256



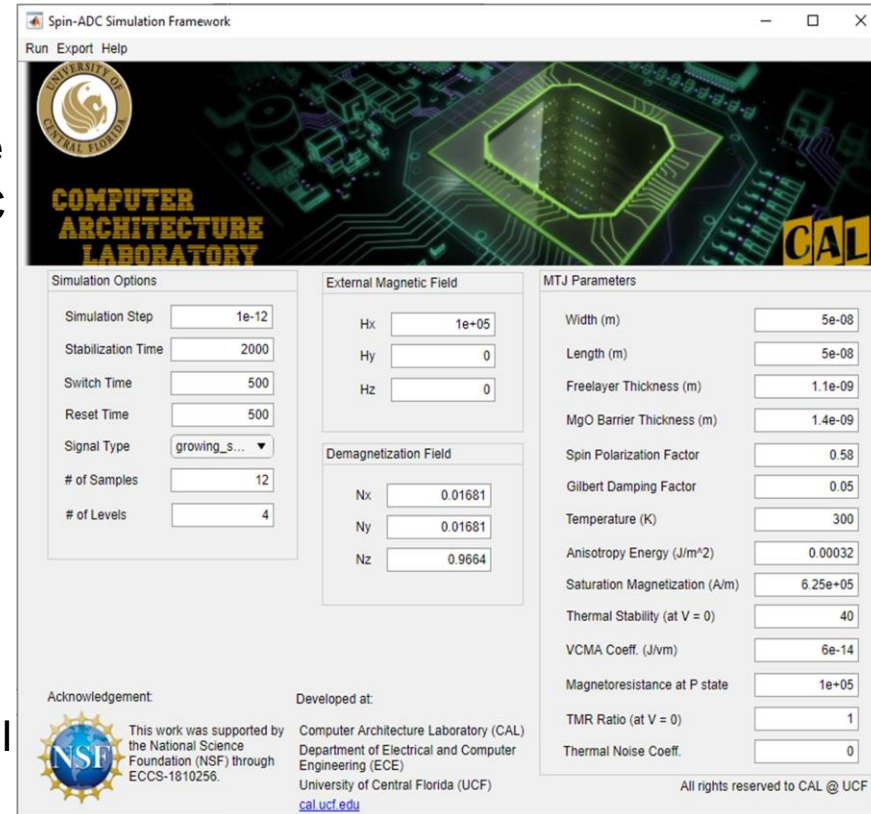
My Proposed Approach

AIQ Simulation Framework^{1,2,3}

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Simulation

Functionalities of proposed Simulation Framework:

- Proposed Interactive Simulator provides a Graphical User Interface (GUI) that allows for the modification and insertion of values for Spin-ADC simulations
- Default parameter values reflect simulation cases used in [S. Salehi, et al., 2018]²
- Vary device parameters for running different simulations with different scenarios
- Run option that compiles all parameters and simulation options to display simulation results
- Simulation results are displayed in a different GUI window displaying different characteristics
- Help option that redirects to various educational resources site for more information



1. G. Camero, S. Salehi, and R. F. DeMara, IEEE ReConfig-2019.

2. S. Salehi, M. Mashhadi, A. Zaeemzadeh, N. Rahnavard, and R. F. DeMara, IEEE JETCAS-2018

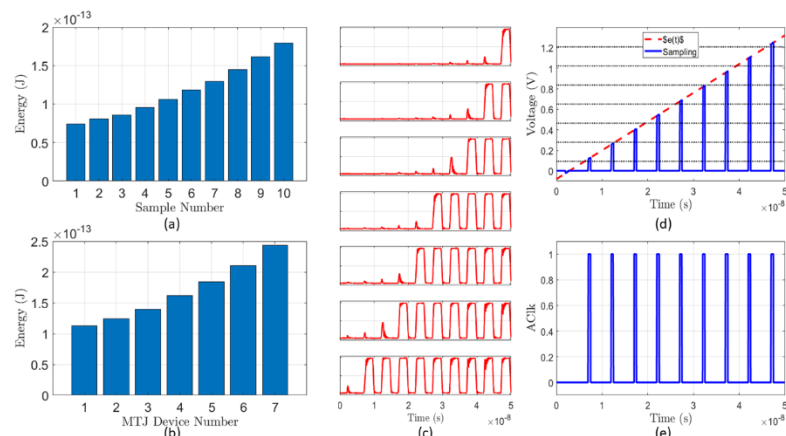
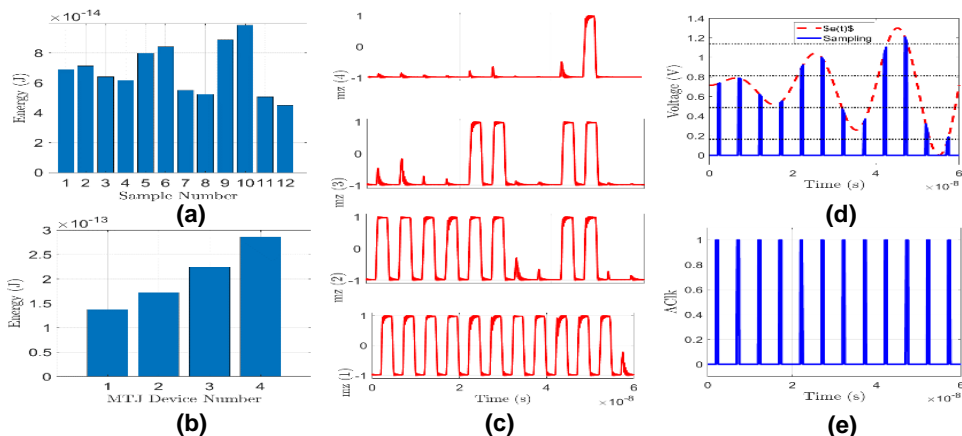
3. This work is funded by NSF-ECCS #1810256



Adaptive & Interactive Framework

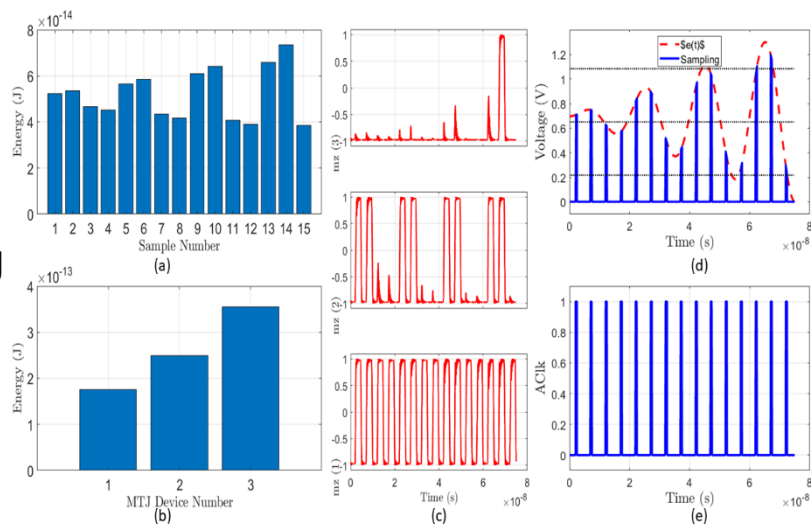
AIQ Simulation Framework^{1,2,3}

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Sample Output Waveforms:

- (a) Depicts energy consumed for each sample
- (b) Illustrates energy consumed by each MTJ
- (c) Shows Magnetization Orientation of each MTJ
- (d) Demonstrates analog input waveform
- (e) Visualizes Sampling Rate



1. G. Camero, S. Salehi, and R. F. DeMara, IEEE ReConfig-2019.
 2. S. Salehi, M. Mashhadi, A. Zaeemzadeh, N. Rahnavard, and R. F. DeMara, IEEE JETCAS-2018
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Educational Outreach Goals

CCSS Website¹

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Simulation

Outreach Objectives:

- Utilize research findings in undergraduate & graduate coursework.
- Develop an interactive tool based on research findings.
- Utilize the proposed tool to engage and attract high school students into STEM-related fields.
- Use educational resources website for explanation and distribution of the proposed interactive tool.

Current Work:

- Youtube Tutorial Video: Simulation Runs with 2-Terminal MTJs
- Youtube Tutorial Video: MTJ Parameters Walkthrough
- Finalize the export option to save the acquired data from simulations in a spreadsheet document

1. G. Camero, S. Salehi, and R. F. DeMara, IEEE ReConfig-2019.
2. S. Salehi, M. Mashhadi, A. Zaeemzadeh, N. Rahnavard, and R. F. DeMara, IEEE JETCAS-2018
3. This work is funded by NSF-ECCS #1810256

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Educational Resources

Spin-ADC Interactive Simulator

- Download [HERE](#)
- SAI-Sim provides a graphical user interface (GUI) that allows for the modification and insertion of values for Spin-ADC Simulations.
- Default parameter values already for simulation purposes based on JETCAS paper featured on this site.
- Control over various simulation options and device parameters for running different simulations with different scenarios.
- Simulation results are displayed in a different GUI window displaying different characteristics.

Tutorials

Paper Resources

Spin-ADC Interactive Simulator was based on the following research papers:

1. S. Salehi, M. Boloursaz Mashhadi, A. Zaeemzadeh, N. Rahnavard, and R. F. DeMara "Energy-Aware Adaptive Rate and Resolution Sampling of Spectrally Sparse Signals Leveraging VCMA-MTJ Devices," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, [pdf]
2. S. Salehi, A. Zaeemzadeh, A. Tatulian, N. Rahnavard and R. F. DeMara, "MRAM-based Stochastic Oscillators for Adaptive Non-Uniform Sampling of Sparse Signals in IoT Applications," accepted to appear in Proceedings of *IEEE Computer Society Annual Symposium on VLSI (ISVLSI'19)*, Miami, Florida, USA, July 15-17, 2019.
3. S. Salehi, R. Zand, A. Zaeemzadeh, N. Rahnavard and R. F. DeMara, "AQuRate: MRAM-based Stochastic Oscillator for Adaptive Quantization Rate Sampling of Sparse Signals," accepted to appear in Proceedings of *ACM Great Lakes Symposium on VLSI (GLSVLSI'19)*, Washington, D.C., USA, May



Spintronic Simulation Framework



For more information regarding the presented simulation tool, please contact us at: <https://cal.ucf.edu/ccss>



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Director of Computer Architecture Lab



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