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SLIM-ADC: Spin-based Logic-In-Memory Analog to Digital Converter leveraging SHE-enabled Domain Wall Motion devices

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ABSTRACT

This paper devises a novel Analog to Digital Converter (ADC) framework for energy-aware acquisition of analog signals with Logic-in-Memory capabilities. The beyond-CMOS hardware architecture has been designed to minimize the overall cost of signal acquisition. Spin-Hall Effect driven Domain Wall Motion (SHE-DWM) devices are utilized to realize the proposed framework called *Spin-based Logic-In-Memory ADC (SLIM-ADC)*. Our simulation results indicate that the proposed SLIM-ADC offers ~ 200 fJ energy consumption on average for each analog conversion or logic operation with up to 1 GHz speed. Furthermore, our results indicate that the proposed SLIM-ADC outperforms other state of the art spin-based ADC designs by offering ~ 5.45 mW improved power dissipation on average. Additionally, a Majority Gate (MG)-based Full-Adder (MG-FA) is implemented using the proposed SLIM-ADC. Our results show that the proposed MG-FA offers ~ 2.9-fold reduced power dissipation on average and ~ 1.7-fold reduced delay on average compared to the state of the art Full-Adder designs reported herein.

1. Introduction

Spin-based devices have been extensively researched as promising companions to CMOS devices. As CMOS scaling trends continue, the need to identify viable approaches for reducing leakage power increases [1]. With attributes of non-volatility, near-zero standby energy, and high density, the Magnetic Tunnel Junction (MTJ) has emerged as a promising alternative post-CMOS technology for embedded memory and logic applications [2–4]. Recent studies have shown that conventional Von-Neumann computing architectures, in which the storing elements are distinct from computing elements, incur challenges created by interconnection and busing demands [5]. These challenges include, but are not limited to, increased static energy consumption, large access latencies, and limited scalability. Recent studies have offered in-memory computing paradigms as a potential solution to these challenges. Use of non-volatile memory devices such as spin-based devices have enabled researchers to design non-Von-Neumann architectures, where processing and memory are integrated [5,6].

Furthermore, there is an increasing demand for energy and area efficient Analog to Digital Converters (ADCs) as the need for integrating the signal acquisition and processing as well as rapid parallel data conversion in sensor nodes has increased [7–9]. One of the main challenges of designing such sensors in CMOS is integrating ADCs in each sensor due to the large area of analog circuits, especially in applications such as image processing where each pixel sensor requires a compact ADC [10,11]. Moreover, another main challenge is the increased static energy consumption due to transistor scaling. Additionally, decreased reliability caused by high process variation can become another major challenge in scaled technology nodes [12].

The above-mentioned challenges have motivated us to devise a framework for efficient acquisition of analog signals utilizing emerging spin-based devices. Herein, we propose a spin-based intermittent quantizer with logic computation capabilities. The proposed architecture, called Spin-based Logic-In-Memory ADC (SLIM-ADC), utilizes Spin-Hall Effect driven Domain Wall Motion (SHE-DWM) devices to provide fast quantization of analog signals in a novel energy-efficient fashion as well as realizing intrinsic logic operations. By leveraging non-volatility, SLIM-ADC can reduce energy consumption via instant off/on operation without the use of backup storage.

The remainder of this paper is organized as follows: A general background and related work are provided in Section 2 and a realization of the acquisition method utilizing the SHE-DWM devices is presented in Section 3. Section 4 provides the simulation results. Finally, Section 5 concludes the paper.

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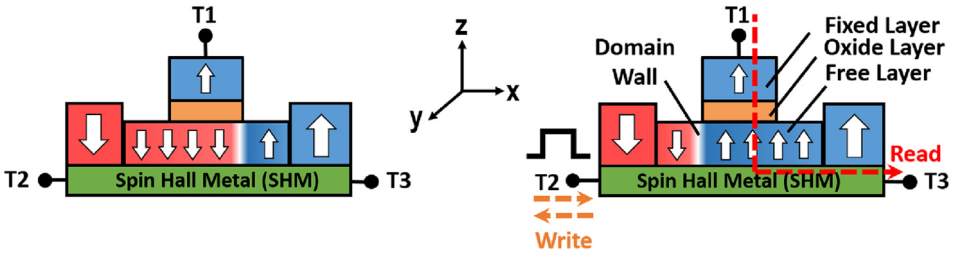

Fig. 1. SHE-enabled Domain Wall Motion device structure.

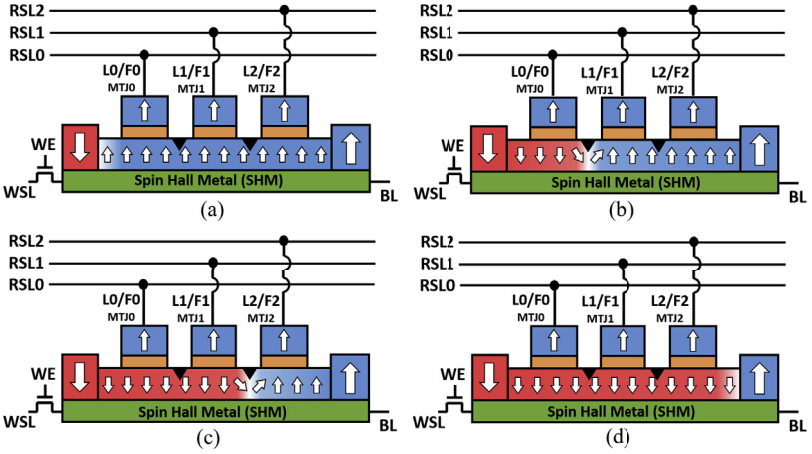

Fig. 2. The proposed SLIM-ADC device in (a) 000, (b) 100, (c) 110, and (d) 111 modes.

2. Background and related work

In recent studies, researchers have exploited the use of emerging devices for signal processing applications. In particular, they have explored designing ADCs using emerging devices such as SHE-MTJ [13], Domain Wall Motion (DWM) [14,15], and Racetrack Memory [16]. The basic concept of spin-based devices is to control the spin of electrons in a ferromagnetic solid-state nano-device. Fig. 1 shows a SHE-DWM device [17,18]. The non-volatile MTJ consists of a Ferromagnetic (FM) layer, which is called the fixed-layer, a FM nano-wire layer, which is called the free-layer, a tunneling oxide layer between the fixed-layer and the free-layer, and a heavy metal to realize Spin-Hall assisted switching. FM layers could be aligned in two different magnetization configurations according to the position of the Domain Wall (DW), Parallel (P) and Anti-Parallel (AP). Accordingly, the MTJ exhibits low resistance (R_P) or high resistance (R_{AP}) states, respectively [17]. The read and write process for the memory cells are like SHE devices. Based on Spin-Transfer Torque (STT) switching principles, the P or AP state of the SHE-DWM device is configured by means of the bidirectional current that passes through the Spin-Hall heavy Metal (SHM) from terminal T1 to terminal T3, I_{SHE}. When the I_{SHE} is applied, a strong spin-orbit coupling is generated, which results in generation of a spin current, I_{Spin}, along the z-axis of the Cartesian coordinate system and perpendicular to the I_{SHE} current [18]. The DW will move if I_{SHE} exceeds the critical current, I_C.

Additionally, in order to read the data stored in these devices, a Sense Amplifier (SA) [2] is used to sense the difference between the resistance of the SHE-DWM device that is used to store the data and a reference MTJ device with a known resistance. Terminals T2 and T3 are used during the read operation, meaning that the read and write paths are separate, which is one of the reasons for high reliability of these devices regarding read disturbance failures. The main reason for using SHE-DWM devices is due to slow and high energy switching of DWM devices alone. Utilizing SHE approach will help reduce the write energy consumption and increase the DW velocity. Conventionally the DWM was achieved using STT which could switch the domain wall due to the coupling between local magnetic moments of the DW and spin-polarized currents. However, it has been practically shown in recent studies that SHE-DWM devices offer significantly lower energy consumption and faster switching [17]. The spin current, I_{Spin}, generated due to the charge current applied through the SHM, I_{SHE}, can be described using the following equations:

$$I_{Spin} = \theta_{SHM} \times \frac{A_{Spin}}{A_{SHM}} \times I_{SHE} \times \sigma \tag{1}$$

$$A_{Spin} = L_{DW} \times W_{DW} \tag{2}$$

$$A_{SHM} = W_{SHM} \times t_{SHM} \tag{3}$$

$$\sigma = 1 - sech(\frac{t_{SHM}}{\lambda_{sf}}) \tag{4}$$

where, L_{DW} and W_{DW} are the length and width of the DW free-layer, W_{SHM} and t_{SHM} are the width and thickness of the SHM, θ_{SHM} is the spin-Hall angle, and λ_{sf} is the spin flip length.

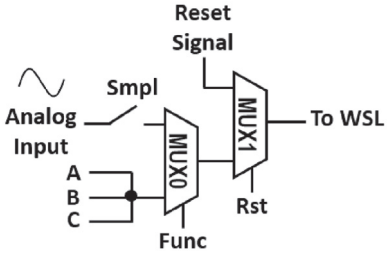

Fig. 3. The proposed write circuit for the SLIM-ADC device.

Table 1
The Signaling of the SLIM-ADC device for read and write operations.

Operation	WSL	RSL	WE	RE	BL
Reset	From write circuit	Hi-Z	1	0	1
Write	From write circuit	Hi-Z	1	0	0
Read	0	From SA	0	1	0

Table 2
The SLIM-ADC's bit encoding for ADC operation.

MTJ0/L0	MTJ1/L1	MTJ2/L2	Encoded Bits
0	0	0	0 0
1	0	0	0 1
1	1	0	1 0
1	1	1	1 1

Table 3
The truth table for the 3-input logic operations.

A	B	C	F0=OR(A,B,C)	F1 = MG(A,B,C)	F2 = AND(A,B,C)
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	1	1	1

Table 4
The truth table for the 2-input logic operations.

A	B	C/Bias	F0=OR(A,B)	F1 = AND(A,B)
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	1	1

3. Spin-based Logic-In-Memory Analog to Digital Converter (SLIM-ADC)

Our proposed SLIM-ADC design leveraging SHE-DWM devices is shown in Fig. 2. Our proposed dual-mode device is capable of implementing ADC operations as well as logical operations. The MTJ0, MTJ1, and MTJ2 each can represent a quantization level referred to as L0, L1, and L2 as shown in Fig. 2, in order to quantize the analog input signal. Additionally, each of these MTJ devices can represent a different function such as 3-input OR gate, 3-input Majority Gate (MG), and 3-input AND gate, shown in Fig. 2 as F0, F1, and F2, respectively. The proposed write circuit used for the SLIM-ADC device is illustrated in Fig. 3. Since there are notches [19] in the magnetic domain, in order to move the DW, the input requires an appropriate current magnitude and direction. Furthermore, the signals used to activate the read and write operations of the SLIM-ADC device are listed in Table 1. One of the main contributions of the proposed SLIM-ADC devices is their tolerance to intermittency which enables these devices to save energy by going to standby mode when there is no ADC or logic operation requested. Moreover, the instant-on feature of these devices allows them to resume normal operation without loss of data stored in the MTJs.

3.1. ADC mode

As depicted in Fig. 3, when the **`Func`** signal for MUX0 is set to 1, the device will be in ADC mode. ADC mode has three simple steps: 1) reset, 2) conversion, and 3) read-out. During the reset state, the **`Rst`** signal of MUX1 will be set to 1 and the DW will be pushed all the way to the beginning of the magnetic domain (leftmost location) to reset and prepare the device for the conversion state. As shown in Fig. 3, during the conversion state, the **`Smpl`** signal will be enabled for a short period to sample the analog input signal and the **`Rst`** signal of MUX1 will be set to 0 to allow the sampled analog input signal to move the DW, depending on the input signal's magnitude. During the read-out state, using the read operation and SAs presented in Ref. [2], we can read the values stored in all 3 MTJs, and based on their resistance values, find the digital output encoded using 3 levels to realize a 2-bit ADC operation as shown in Fig. 2, where L0, L1, and L2 refer to Level 0, Level 1, and Level 2, respectively. During the read operation one of the 000, 100, 110, or 111 states will be achieved that can be encoded into two bits as shown in Table 2.

3.2. Logic-In-Memory mode

Furthermore, when the **`Func`** signal for MUX0 is set to 0, the device will be in logic operation mode, as illustrated in Fig. 3. The logic operation has also three steps: 1) reset, 2) computation, and 3) read-out. During the reset state, which is the same as ADC mode, the **`Rst`** signal of MUX1 will be set to 1 and the DW will be pushed all the way to the beginning of the magnetic domain (leftmost location) to reset and prepare the device for the computation state. As depicted in Fig. 3, after the reset state, the input currents of A, B, and C will be applied during the computation state for logic operation. Based on the current magnitude applied through the inputs A, B, and C, the DW will move. Finally, in the read-out state, the output of each MTJ will provide a different function as shown in Fig. 2. The proposed device is designed so that F0 provides a 3-input OR gate, OR(A,B,C), F1 provide a 3-input Majority gate, MG(A,B,C), and F2 provides a 3-input AND gate, AND(A,B,C), as listed in Table 3. Additionally, one of the inputs can be used as a bias to achieve 2-input OR and AND gates. Herein, if we consider input C as the bias and connect it to logic 0, then MTJ0 will provide OR(A,B) as F0, and MTJ1 will provide AND(A,B) as F1, as listed in Table 4.

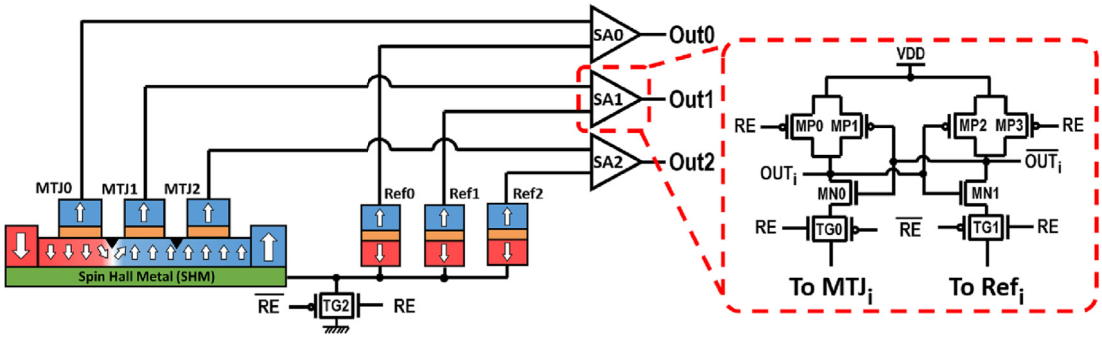

Fig. 4. The proposed SA circuit for the SLIM-ADC device ($i = \{0, 1, 2\}$).

Table 5
Circuit parameters and constants with their corresponding values for the SHE-DWM device model. The values are taken from Refs. [17,20,21].

Parameter/Constant	Description	Default Value
M_s	Saturation Magnetization	6.8×10^5 A/m
K_u	Initial Interfacial PMA energy	3.5×10^5 J/m^3
α	Gilbert Damping Factor	0.03
t_{ox}	Oxide-layer Thickness	1 nm
A_{ex}	Exchange Stiffness	1.1×10^{-11} J/m
ρ	Resistivity of Magnet	170 Ωnm
RA	MTJ Resistance Area Product	2.38 Ωμm^2
$(L \times W)_{MTJ}$	MTJ Dimensions	20×20 nm^2
$(L \times W \times t)_{DW}$	DW Nano-wire Dimensions	$100 \times 20 \times 2.8$ nm^3
$(L \times W \times t)_{SHM}$	SHM dimensions	$120 \times 20 \times 2.8$ nm^3
MTJ_i	MTJ Resistance in [P, AP] States	[3.2, 6.4] KΩ
Ref_i	Reference Cell Resistance	4.8 KΩ
ρ_{SHM}	Resistivity of SHM (W)	200 μΩcm^2
θ_{SHM}	Initial Spin-Hall angle	0.3
TMR_{AP}	Tunnel Magneto Resistance	100%
P	Spin Polarization	0.6
λ_{sf}	Spin Flip Length	1.5 nm

3.3. Sense Amplifier (SA) circuit for the read operation

The Sense Amplifier (SA) circuit shown in Fig. 4 is used to read the data of the three MTJ devices, namely MTJ0, MTJ1, and MTJ2, simultaneously. The read operation is comprised of two steps: pre-charge and sensing. During the pre-charge step, the RE signal is connected to the logic 0, which turns on *MP*0 and *MP*3 transistors and causes Transmission Gates (TGs), *TG*0, *TG*1, and *TG*2, to turn off and as a result the output nodes of each SA, referred to as OUT_i and $\overline{OUT_i}$ in Fig. 4, are pre-charged to VDD. During the sensing step, the RE signal is connected to logic 1, which causes *TG*0, *TG*1, and *TG*2 to turn on and as a result the output nodes of each SA, referred to as OUT_i and $\overline{OUT_i}$ in Fig. 4, start to discharge to the ground. According to the difference in the resistance states of the MTJ_i and Ref_i in each SA, one of the two output nodes, OUT_i and $\overline{OUT_i}$, discharges more rapidly, leading the other output to charge to VDD [2]. All of the reference cells, Ref_0, Ref_1, and Ref_2, share the same dimensions and resistance values. The dimensions are set so that the resistance values of the reference cells hold a value between the P and AP states of the MTJs used with the SHE-DW. All of the reference cells, Ref_0, Ref_1, and Ref_2, share the same dimensions and resistance values. The dimensions are set so that the resistance values of the reference cells hold a value between the P and AP states of the MTJs used with the SHE-DW in order to achieve a sufficient sensing margin during the read operation.

4. Simulation framework, results, and analysis

In order to accurately simulate the behavior of the proposed SLIM-ADC design, we have extracted the values used in Refs. [17,20,21]. The Domain Wall Simulator presented in Ref. [20] are used along with SPICE simulation with the 22 nm Predictive Technology Model (PTM) [22], in order to analyze the behavior of the SHE-DWM devices proposed herein utilizing the parameters listed in Table 5.

The modeling of the SHE-DWM can be realized through modifying the Landau-Lifshitz-Gilbert (LLG) equations as shown below [21]:

$$\frac{d\vec{m}}{dt} = -\gamma \vec{m} \times \vec{H}_{eff} + \alpha \vec{m} \times \frac{d\vec{m}}{dt} + \vec{\tau}_{stt} + \vec{\tau}_{sot}, \tag{5}$$

where, $\vec{m}$ is the magnetization vector of the DW's free-layer $\{m_x, m_y, m_z\}$, γ is the gyromagnetic ratio, α is the Gilbert damping factor, $\vec{H}_{eff}$ is the effective magnetic field vector derived from the energy density of the system, τ_{stt} is the Spin-Transfer Torque (STT) factor, and τ_{sot} is the Spin-Orbit Torque (SOT) factor. Additionally, H_{eff} can be described as [21]:

$$\vec{H}_{eff} = \frac{-1}{\mu_0 M_s} \times \frac{\delta \epsilon_{DM}}{\delta \vec{m}}, \tag{6}$$

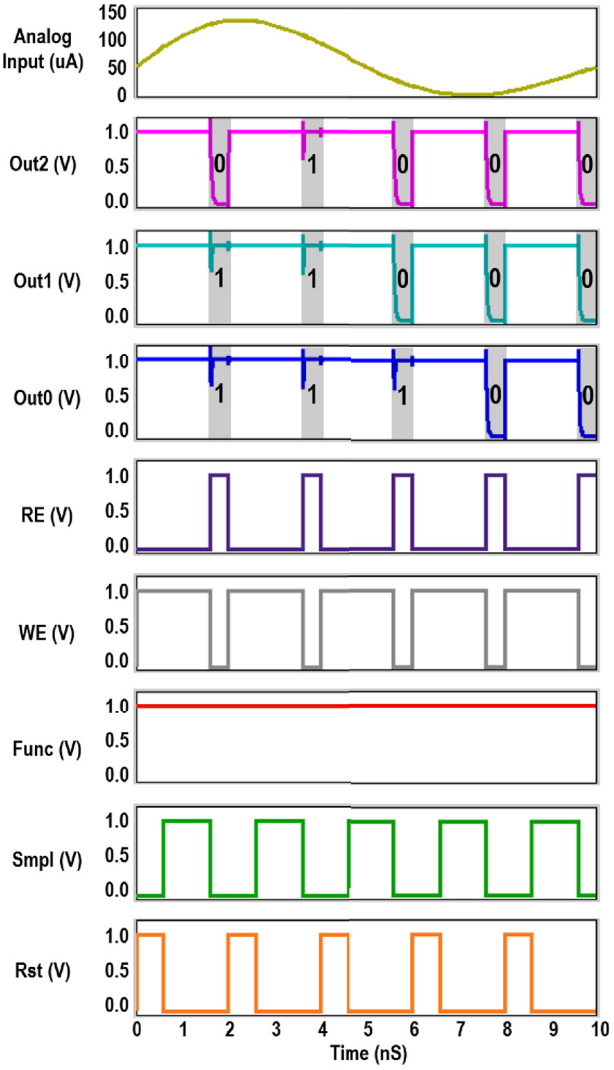

Fig. 5. Simulation waveforms for the proposed SLIM-ADC device.

Table 6
Comparison with prior low-resolution ADC designs. (N/A: Data Not Available in the referenced manuscript).

Design	Technology	Resolution in Bits	Power	Maximum Bandwidth Frequency	Energy per Sample
[23]	CMOS	4-bit	30 mW	20 MHz	5 pJ
[24]	CMOS	3-bit	3.1 mW	2 GHz	0.27 pJ
[25]	SHE-MTJ	3-bit	1.9 mW	500 MHz	0.48 pJ
[14]	DWM	5-bit	3.4 mW	500 MHz	3.5 pJ
[15]	DWM	3-bit	0.22 mW	200 MHz	N/A
			1.44 mW	500 MHz	N/A
			6.56 mW	1 GHz	N/A
[16]	Racetrack DWM	8-bit	96.5 µW	20 MHz	21 fJ
SLIM-ADC	**SHE-DWM**	**2-bit**	**285.87 µW**	**500 MHz**	**79.71 fJ**
			549.51 µW	**1 GHz**	**79.52 fJ**

$$\epsilon_{DM} = -D[m_z \nabla \cdot \vec{m} - (\vec{m} \cdot \nabla) m_z] \quad \text{if } t_{DW} \ll L_{DW} \ \& \ W_{DW}, \tag{7}$$

where, μ_0 is the vacuum permeability, M_s is the Saturation Magnetization, ϵ_{DM} is the Dzyaloshinskii-Moriya Interaction (DMI) energy density, and D is the DMI intensity parameter. As a result, the effective DMI field can be described as below [21]:

$$\vec{H}_{DM} = \frac{-2D}{\mu_0 M_s} \times [\frac{\partial m_z}{\partial x}\vec{u}_x + \frac{\partial m_z}{\partial y}\vec{u}_y - (\frac{\partial m_x}{\partial x}\vec{u}_x + \frac{\partial m_y}{\partial y}\vec{u}_y)\vec{u}_z]. \tag{8}$$

Furthermore, assuming that $\hbar$ is the reduced Planck constant, P is the STT polarization factor, j_a is the driving current density, e is the elementary electron charge, μ_B is the Bohr magneton, θ is the initial spin-Hall angle, η is the non-adiabatic Rashba term, ξ is the dimensionless non-adiabatic parameter, α_R is the Rashba parameter, and $\vec{H}_R$ is the effective Rashba field, the STT and SOT factors can be described as below [21]:

$$\vec{\tau}_{stt} = (j_a \frac{\mu_B P}{e M_s}) \times (\vec{u}_x \cdot \nabla)\vec{m} - (j_a \frac{\mu_B P}{e M_s}) \times \xi \vec{m} \times (\vec{u}_x \cdot \nabla)\vec{m}, \tag{9}$$

$$\vec{\tau}_{sot} = -\gamma \vec{m} \times \vec{H}_R + \eta\gamma\xi \vec{m} \times (\vec{m} \times \vec{H}_R) - \gamma \vec{m} \times (\vec{m} \times H_{SH}\vec{u}_y), \tag{10}$$

$$\vec{H}_R = \frac{\alpha_R P}{\mu_0 \mu_B M_s}(\vec{u}_z \times \vec{j}_a) = \frac{\alpha_R P j_a}{\mu_0 \mu_B M_s}\vec{u}_y, \tag{11}$$

$$H_{SH} = \frac{\hbar \theta_{SH} j_a}{\mu_0 2eM_s t_{DW}} = \frac{\mu_B \theta_{SH} j_a}{\gamma 2eM_s t_{DW}}, \tag{12}$$

Authors in Ref. [20] have utilized the modeling approach described in Ref. [21] to implement a standalone one-dimensional DWM simulator. This model takes STT, SOT, and DMI fields into account [20]. According to our results, if $j_a \simeq 0.75 \times 10^{12}$ A/m^2 is applied, the DW will move to the first notch within 1 ns, if $j_a \simeq 1.44 \times 10^{12}$ A/m^2 is applied, the DW will move to the second notch within 1 ns, and if $j_a \simeq 2.08 \times 10^{12}$ A/m^2 is applied, the DW will move all the way to the end of the magnetic domain within 1 ns. Fig. 5 depicts sample simulation waveforms for the proposed SLIM-ADC device. According to our results, the energy consumption of each ADC or logic operation on average is ~ 201.48 fJ, which on average includes ~ 117.94 fJ for the reset operation, ~ 79.70 fJ for the sampling/computing operation, and ~ 3.84 fJ for the read operation. Considering 0.6ns for the reset operation, 1ns for the sample/compute operation, and 0.4ns for the read operation, the overall operation time is 2 ns, which means the proposed SLIM-ADC device can perform ADC or logic operations with 500 MHz frequency.

Faster ADC and logic operations can be achieved by increasing the input current corresponding to reset and sample/compute operations, however this will elevate the power dissipation. In order to increase the speed of the proposed SLIM-ADC device to be able to perform ADC or logic operations with 1 GHz frequency, the reset operation is required

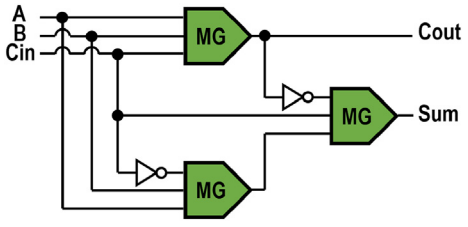

Fig. 6. Proposed 1-bit MG-FA circuit implemented utilizing the SLIM-ADC devices.

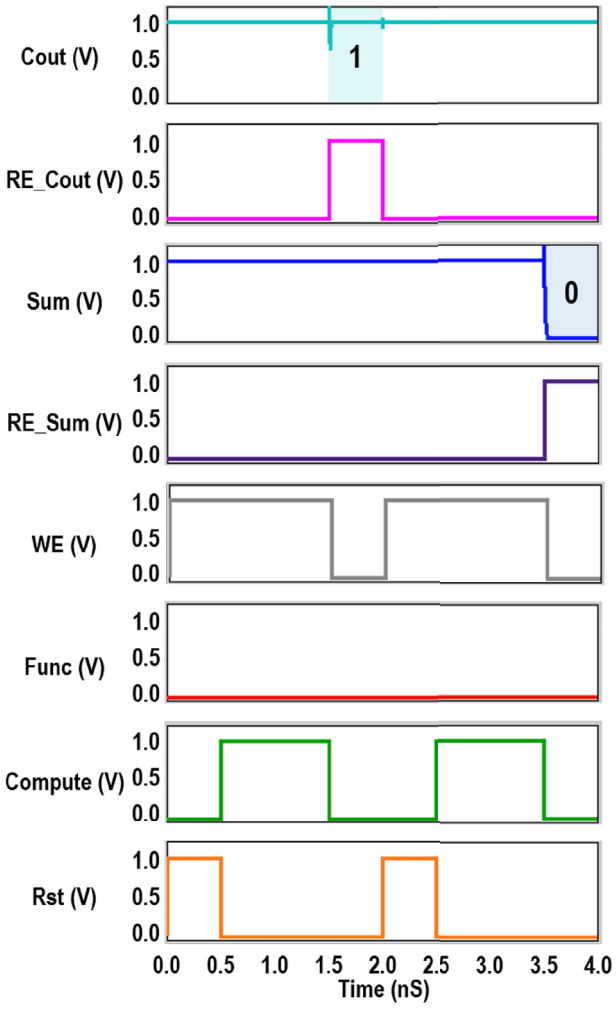

Fig. 7. Simulation waveforms for the proposed 1-bit MG-FA circuit implemented utilizing the SLIM-ADC devices with inputs A = 1, B = 0, Cin = 1.

Table 7
Comparison with prior Full-Adder designs. (*The values are taken from Ref. [26]).

Design	Technology	Power	Delay	Energy per bit
[27]*	CMOS	2 mW	2.2ns	4 pJ
[27]*	STT-MTJ	2.1 mW	10.2ns	4.2 pJ
[26]*	SHE-MTJ	0.71 mW	7ns	4.3 pJ
[28]	DWM	1.364 mW	2.54ns	1.4 pJ
[29]	STT-MTJ	0.315 mW	2.1ns	6.3 pJ
[30]	Racetrack DWM	0.432 mW	3.03ns	1.3 pJ
SLIM-ADC	**SHE-DWM**	**589.95 µW**	**2ns (1 GHz)**	**0.6 pJ**
		302.22 µW	**4ns (500 MHz)**	**0.6 pJ**

to be done in 0.3 ns, sample/compute operation is required to be done in 0.5 ns, and read operation requires to be done in 0.2 ns. Furthermore, according to our results, if $j_a \simeq 1.57 \times 10^{12}$ A/m^2 is applied, the DW will move to the first notch within 0.5 ns, if $j_a \simeq 2.85 \times 10^{12}$ A/m^2 is applied, the DW will move to the second notch within 0.5 ns, and if $j_a \simeq 4.1 \times 10^{12}$ A/m^2 is applied, the DW will move all the way to the end of the magnetic domain within 0.5 ns. In this case, the energy consumption of each ADC or logic operation is equal to ~ 196.65 fJ on average, which includes ~ 117.1 fJ for the reset operation, ~ 79.52 fJ for the sampling/computing operation, and ~ 0.03 fJ for the read operation.

In Table 6, we compare the performance of the developed SLIM-ADC device with other low-resolution ADC architectures that utilize CMOS or emerging spin-based technologies. It can be observed that the proposed SLIM-ADC device provides fast and energy-efficient analog to digital conversion compared to state of the art ADC designs. In particular, the proposed SLIM-ADC operating in 1 GHz frequency, in most cases outperform other designs listed in Table 6 in terms of power dissipation by ~ 5.3 mW on average. Moreover, the proposed SLIM-ADC design improves the power dissipation of the sampling in 500 MHz frequency by ~ 5.6 mW on average compared to most of the designs provided in Table 6.

Moreover, a 1-bit MG-based Full-Adder (MG-FA) circuit is implemented utilizing the proposed SLIM-ADC devices using the circuit shown in Fig. 6. According to our results, the power dissipation of the proposed SLIM-ADC-based MG-FA in 1 GHz frequency is equal to 589.95 µW and the result of the addition will be ready within 2 ns. Furthermore, the power dissipation of the proposed SLIM-ADC-based MG-FA in 500 MHz frequency is equal to 302.22 µW and the result of the addition will be ready within 4 ns. The output waveform of the 1-bit MG-FA circuit using the proposed SLIM-ADC devices is shown in Fig. 7.Table 7 compares the performance of the developed SLIM-ADC-based MG-FA with other FA designs that utilize CMOS or emerging spin-based technologies. It can be observed that the proposed SLIM-ADC-based MG-FA operating in 1 GHz frequency outperforms the other FA designs listed in Table 7 in terms of power dissipation by 2.7-fold on average. Additionally, the proposed SLIM-ADC MG-FA offers faster FA operation by 3.2-fold on average compared to other FA designs listed in Table 7. Furthermore, the proposed SLIM-ADC MG-FA offers ~ 2-fold and ~ 3.8-fold reduced power dissipation on average in 1 GHz and 500 MHz operating speeds, respectively, and provides ~ 2.3-fold and ~ 1.13-fold delay improvement on average in 1 GHz and 500 MHz operating speeds, respectively, compared to other emerging spin-based FA designs listed in Table 7.

Previous results indicate that for a conventional 2-bit CMOS ADC requires 49 transistors [31] and 1-bit CMOS FA requires 42 transistors [27], while our proposed SLIM-ADC can perform 2-bit ADC and 1-bit FA operation with 90 total transistors and 6 total MTJs. Thus, the device count for implementing a single ADC and FA circuit is comparable with the conventional CMOS-based approaches. However, compared to the conventional Logic In Memory (LIM) and ADC approaches, the area of the proposed SLIM-ADC is reduced, since an array of SAs is shared among the entire column of SLIM-ADC devices and an array of write circuits is shared among the entire row of SLIM-ADC devices. Hence, there is no need for a distinct SA and write circuit per device. Furthermore, the proposed SLIM-ADC device is capable of both logic and ADC operations while conventional approaches are only capable of performing one operation, either logic or ADC. Additionally, according to our results, the proposed SLIM-ADC consumes ~ 0.2 µW leakage power which is negligible compared to CMOS designs which is around ~ 1 nW [27].

5. Conclusion

To advance energy-sparing sampling methods, a novel framework for efficient and intelligent computing approach through the integration of resource allocation and spin-based devices is introduced. The utility of SHE-DWM devices within the proposed SLIM-ADC architecture is demonstrated to realize rapid and more energy-efficient sampling while achieving reduced area footprint compared to conventional CMOS designs. Moreover, SLIM-ADC takes a step towards the realization of non-Von-Neumann architectures via in-memory computation utilizing SHE-DWM devices. According to our simulation results, the proposed SLIM-ADC offers ~ 200 fJ energy consumption on average for each analog conversion or logic operation with up to 1 GHz speed. Furthermore, our results indicate that the proposed SLIM-ADC outperforms other state of the art spin-based ADC designs by offering ~ 5.5 mW improved power dissipation on average. Additionally, a Majority Gate (MG)-based Full-Adder (MG-FA) is implemented using the proposed SLIM-ADC. Our results show that the proposed MG-FA offers ~ 2-fold and ~ 3.8-fold reduced power dissipation on average in 1 GHz and 500 MHz operating speeds, respectively, compared to the state of the art Full-Adder designs reported herein. Additionally, according to our results, the proposed MG-FA provides ~ 2.3-fold and ~ 1.13-fold reduced delay on average in 1 GHz and 500 MHz operating speeds, respectively, compared to the state of the art Full-Adder designs reported herein.

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