Energy-Aware Adaptive Rate and Resolution Sampling of Spectrally Sparse Signals Leveraging VCMA-MTJ Devices

Soheil Salehi, *Student Member, IEEE,* Mahdi Boloursaz Mashhadi, *Student Member, IEEE,* Alireza Zaeemzadeh, *Student Member, IEEE,* Nazanin Rahnavard, *Member, IEEE,* and, Ronald F. DeMara, *Senior Member, IEEE*

***Abstract*—This paper devises a novel adaptive framework for energy-aware acquisition of spectrally-sparse signals. The adaptive quantized Compressive Sensing (CS) techniques, beyond-Complementary Metal Oxide Semiconductor (CMOS) hardware architecture, and corresponding algorithms which utilize them have been designed concomitantly to minimize the overall cost of signal acquisition. First, a spin-based *Adaptive Intermittent Quantizer (AIQ)* is developed to facilitate the realization of the adaptive sampling technique. Next, a framework for smart and adaptive determination of the sampling rate and quantization resolution based on the instantaneous signal and hardware constraints is introduced. Finally, signal reconstruction algorithms which process the quantized CS samples are investigated. Simulation results indicate that an AIQ architecture using a spin-based quantizer incurs only 20.98μW power dissipation on average using 22nm technology for 1 to 8 bits uniform output. Furthermore, in order to provide 8-bit quantization resolution, 85.302μW maximum power dissipation is attained. Our results indicate that the proposed AIQ design provides up to 6.18mW power savings on average compared to other adaptive rate and resolution CMOS-based CS Analog to Digital Converter (ADC) designs. Additionally, the Mean Square Error (MSE) values achieved by the simulation results confirm efficient reconstruction of the signal based on the proposed approach.**

***Index Terms*—Adaptive sampling rate; Adaptive quantization resolution; Compressive sensing; Beyond-CMOS devices; Magnetic Tunnel Junction (MTJ).**

I. Introduction

ADAPTIVE signal acquisition and conversion circuits using emerging spin-based devices offer a new and highly-favorable range of accuracy, bandwidth, miniaturization, and energy trade-offs. The use of such approaches specifically targets new classes of Analog to Digital Converter (ADC) designs providing *sampling rate* (SR) and *quantization resolution* (QR) adapted during acquisition by a cross-layer strategy considering both signal and hardware specific constraints.

Prior works on adaptive rate and resolution ADCs [1–8] have optimized the rate/resolution trade-off assuming a low-pass signal model and utilizing Complementary Metal Oxide Semiconductor (CMOS) technology. However, in this work, we use the theory of Compressive Sensing (CS) [9, 10] and spin-based devices [11–24] to advance beyond these limitations. Compressive sensing is a modern signal acquisition paradigm that aims to measure sparse signals close to their *information rate* rather than their *Nyquist rate*. This is specifically critical for *spectrally sparse wide-band signals* in which conventional sampling becomes impractical due to challenges associated with building sampling hardware that operates at prohibitively high Nyquist rates.

Quantized CS [25–28] aims at addressing the existing trade-off between the number of measurements and the number of bits used to quantize each measurement for a fixed bit budget. Although this trade-off has been studied previously [25–28], adaptive optimization of the SR and QR during signal acquisition has not been investigated. Moreover, despite the fundamental theoretical discoveries in this field, quantized CS techniques are mostly designed and implemented *oblivious* to the specifics and limitations of the hardware platform that performs the sampling/acquisition. In other words, in the rate/resolution trade-off, both signal dependent constraints (e.g., sparsity and noise level) and hardware dependent constraints (e.g., energy, bandwidth, and battery capacity) play an important role and as these constraints vary during signal acquisition, dynamic and cross-layer optimization of SR and QR is desirable for efficient signal acquisition. While adaptive SR and QR seem to be viable approaches from the signal processing and algorithmic point of view, the actual implementation of them requires a hardware platform that can adapt itself to these variations.

The above-mentioned challenges motivated us to devise an adaptive framework for efficient acquisition of spectrally sparse signals utilizing emerging spin-based devices. In the first contribution herein, we propose a Spin-based Adaptive Intermittent Quantizer (AIQ) to perform adaptive signal sampling and quantization. AIQ utilizes Voltage-Controlled Magnetic Anisotropy Magnetic Tunnel Junction (VCMA-MTJ) devices to provide fast SR and adaptive QR in a novel energy-efficient fashion. By leveraging non-volatility, a spin-based AIQ can reduce energy consumption via instant off/on operation without use of a backing store.

The second contribution herein focuses on investigating the trade-offs between SR and QR under power and bandwidth constraints using dynamic optimization of SR and QR. The energy consumption, hardware limitations, and specifics of the underlying sampler and quantizer become central to system

Soheil Salehi, Mahdi Boloursaz Mashhadi, Alireza Zaeemzadeh, Nazanin Rahnavard, and Ronald F. DeMara are with the Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL, 32816, USA. corresponding author e-mail: soheil.salehi@knights.ucf.edu.

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optimization. Specifically, computationally efficient signal reconstruction algorithms are developed to reconstruct the original signal from its non-uniform quantized CS measurements. It not only reduces the computational complexity of the proposed algorithm in comparison with the batch-based reconstruction algorithms proposed in the Quantized Compressive Sensing (QCS) literature, but also eliminates the corresponding frame processing delay. This is further explained in Section IV-C.

The proposed beyond-CMOS hardware architecture and corresponding adaptive quantized CS techniques are considered in synergy with each other. Together these are used to minimize the *overall cost of signal acquisition* which is later formulated as a combination of the amount of dynamic energy consumed in hardware for acquisition (energy constraint) and the number of bits acquired for each frame (bandwidth constraint) within the reconstruction error (MSE) for a spectrally-sparse input signal.

The key innovations and contributions of our developed approach are listed below:

- A novel framework for efficient and intelligent sensing through integration of resource allocation, quantized compressive sensing, and spin-based devices is introduced,
- SR and QR trade-offs under resource constraints are studied and an energy-aware adaptive SR / QR optimization framework to tune the sampling rate and quantization resolution is innovated,
- Novel sampling and reconstruction algorithms are developed in the context of adaptive quantized CS,
- The utility of VCMA-MTJ devices within the proposed AIQ architecture is demonstrated to realize faster and more energy-efficient sampling and signal processing while achieving reduced area footprint compared to conventional CMOS designs, and
- An energy equation for the SR / QR optimization process is derived.

The remainder of this paper is organized as follows. A general introduction of the proposed acquisition approach is provided in Section II. A realization of the acquisition method utilizing the spin-based VCMA-MTJ devices is presented in Section III. The proposed energy-aware quantized CS approach is introduced in Section IV. Section V provides the simulation results and comparisons. Finally, Section VI concludes the paper.

II. Proposed Cross-Layer Approach

In this paper, we develop a novel cross-layer device/circuit/architecture design for adaptive signal sampling, reconstruction, and the enabling hardware for energy-efficient acquisition of wide-band spectrally sparse signals. First, a framework for smart and adaptive determination of the sampling rate and quantization resolution based on the instantaneous signal and hardware constraints is introduced. Furthermore, computationally effective signal reconstruction algorithms from the quantized CS samples are investigated. Second, we develop a spin-based *Adaptive Intermittent Quantizer* (AIQ) to facilitate the realization of the adaptive sampling proposed herein. Fig. 1(a) shows the system-level diagram for our proposed design. In this figure, the input signal $x(t)$ is compared with the estimate signal $\widehat{x}(t)$. The error signal $e(t)$ then goes through our proposed ***AIQ*** which samples each frame of the input at a specific sample rate, i.e. frame n_f is sampled at $t = m\tau^{(n_f)}$, quantized to symbols c_m and subsequently to the corresponding bit stream b_m. Note that $\tau^{(n_f)}$ is the sampling interval, which is adaptively determined for frame n_f of the signal.

To encode the signal more efficiently, $x(t)$ is estimated from b_m in a feedback loop, utilizing a sparsity promoting algorithm in the Sparse Component Estimator (SCE) block. The AIQ later quantizes and encodes the estimation error signal $e(t) = x(t) - \widehat{x}(t)$ to the sequence of bits b_m. Note that at the transmitter, the AIQ block could alternatively encode the input signal $x(t)$ itself, however that would be redundant in the sense that we do not need to encode and transmit part of the signal that is predictable from the previously encoded sequence of bits. In other words, the proposed approach is preferred as it only encodes the unpredictable part of the input signal ($e(t)$) by subtracting the predictable part ($\widehat{x}(t)$). Taking this approach, we observe that the dynamic range of the input $e(t)$ is significantly reduced in comparison with $x(t)$ itself which enables the transmitter to decrease the number of quantization levels and bits needed to encode it and hence further reduces the bandwidth requirement. Utilizing this approach, reconstruction by quantized compressive sensing is still possible at a negligible additional computation overhead as described in Section IV-C. Note that this is a common strategy already used in popular Delta and Sigma-Delta modulation ADCs when the input signal is band-limited. However, it has not been utilized with sparse signals in the context of compressive sensing before. The corresponding receiver block shown in Fig. 1(b) utilizes the same sparsity-promoting algorithm to reconstruct $x(t)$ from the received sequence of erroneous stream of bits denoted by $\hat{b_m}$.

The *adaptive Sample-Rate (SR) / Quantization-Resolution (QR) controller* is a key innovation of our approach. This block optimizes SR ($\frac{1}{\tau^{(n_f)}}$Hz) and the number of digital bits used to quantize each sample (QR) for each frame of the input signal. For that, this block utilizes the signal parameters (e.g., sparsity, noise level) estimated at the previous frame and hardware-level constraints (e.g., energy, bandwidth). This block provides the optimized clock period and bit depth for the next frame of the signal. The same block is present at the receiver to extract bit-depth resolution and the sampling rate from the received sequence of bits. Components of our design are described below.

Spin-based devices have been extensively researched as promising companions to CMOS devices. As CMOS scaling trends continue, the need to identify viable approaches for reducing leakage power increases. With attributes of non-volatility, near-zero standby energy, and high density, Magnetic Tunneling Junction (MTJ) has emerged as a promising alternative post-CMOS technology for embedded memory and logic applications [11–14]. The basic concept of spin-based Non-Volatile Memory (NVM) devices is to control the intrinsic spin of electrons in a ferromagnetic solid-state nano-device. Recent research studies have shown that use of the Voltage-

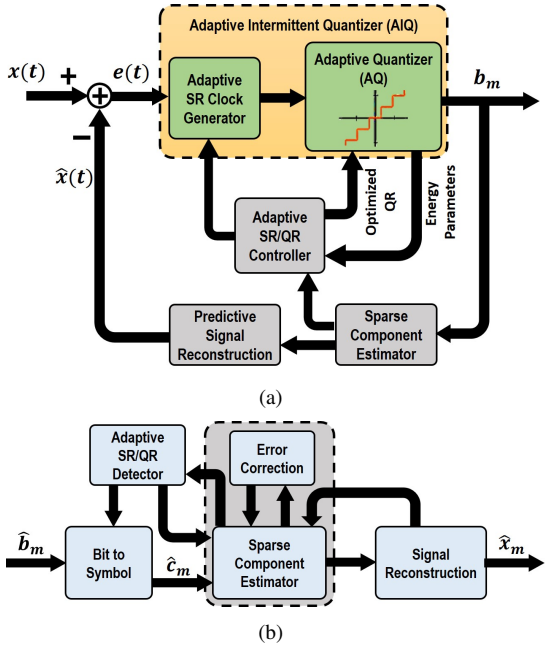


Fig. 1: (a) The system-level block diagram of the proposed signal acquisition and (b) the corresponding reconstruction technique.

Controlled Magnetic Anisotropy (VCMA) effect facilitates the use of an electric field to ease or eliminate the demand of charge current for switching the state of MTJ devices. As a result of using VCMA-MTJ devices, the majority of the dynamic power dissipation caused by ohmic losses and joule heating during the switching of the spin-based devices can be significantly reduced [14–19].

Adaptive Intermittent Quantizer (AIQ): Herein, to implement the adaptive rate/resolution sampling, a recently-developed type of spin-based device, namely the VCMA-MTJ, is utilized to provide faster and more energy-efficient signal sampling and quantization. Previously, emerging spin-based technologies have been explored as an alternative to CMOS technology for embedded and data storage applications due to their non-volatility, near-zero standby energy, and high density. These emerging devices, such as Spin Transfer Torque Magnetic RAM (STT-MRAM) and Spin-Hall Effect Magnetic RAM (SHE-MRAM), have been the focus of the research in recent years [11–14, 20–22]. Using spin-based devices can increase energy efficiency via a significant reduction in leakage energy. Furthermore, these devices offer small area footprint and can be fabricated in 3D stacks on top of baseline CMOS design using the same backend fabrication process. A detailed explanation of this block is provided in Section III.

Sparse Component Estimator (SCE): The quantized Sparse Component Estimator (SCE) block estimates the sparse spectral components from the output bit stream utilizing an iterative algorithm. Unlike the previously proposed batch-based algorithms for quantized compressive sensing [25–28], our proposed algorithm operates only one iteration on each frame of the input by utilizing the previous estimate as an initial value. This way, the computational burden on the signal acquisition block is reduced and the sparse spectral components gradually converge to the actual values across iterations. This block is used at both acquisition and reconstruction phases to predict the signal estimate $\hat{x}(t)$ (in the feedback loop at acquisition). A detailed explanation of this block is provided in Section IV-C.

Adaptive SR/QR Optimization: The concept of energy-aware SR/QR optimization is motivated by the fact that, in any practical scenario, sensing operations need to be able to satisfy the power and bandwidth constraints. Under a bandwidth constraint, the sensing device is constrained by a bit-rate when transmitting or storing the signal. On the other hand, the energy supply might impose strict constraints on the SR and/or QR. Thus, it is desirable to have a system that adapts SR and QR to maximize the sensing performance in the long run, while considering the power and bandwidth constraints. A detailed explanation of this block is later provided in Section IV-D.

III. Intermittent Spin-based Adaptive Quantizer Using VCMA-MTJ Devices

A. Background and Related Work

The basic concept of spin-based devices is to control the spin of electrons in a ferromagnetic solid-state nano-device. Fig. 2 shows a STT-MRAM cell structure using a single transistor, known as "one-transistor-one-MTJ (1T-1R)" configuration [12]. Each bit cell is accessed via the corresponding bit-line within the resident word selected by the word-line. These MTJ devices are constructed with layered pillars of ferromagnetic and insulating materials to utilize magnetic orientations that can be controlled and sensed in terms of electrical signal levels as shown in Fig. 2.

The non-volatile MTJ consists of two Ferromagnetic (FM) layers, which are called the fixed-layer and the free-layer, and one tunneling oxide layer between the two FM layers [12]. FM layers could be aligned in two different magnetization configurations, Parallel (P) and Anti-Parallel (AP). Accordingly, the MTJ exhibits low resistance (R_P) or high resistance (R_{AP}) states, respectively [12]. Based on STT switching principles, the P or AP state of the MTJ is configured by means of the bidirectional current that passes through it, I_{MTJ}, which can readily be produced by simple MOS based circuits. The states of the MTJ are switched when I_{MTJ} exceeds critical current, I_C.

B. VCMA-MTJ Devices for Energy-Efficient Architectures

Although MTJs offer non-volatility, near zero stand-by power dissipation, area efficiency, and fast read operation, their write energy is still significantly higher than volatile switching devices. Thus, it is proposed here to address energy-inefficient and slow write operation by investigating a new approach to modify the switching energy barrier [14]. Due to the current-driven operation of spin-based devices, the majority of the dynamic power dissipation during the switching is caused by ohmic losses and joule heating [15]. In order to solve this issue, researchers have studied the magnetoelectric effect to enable new switching mechanism as an alternative to conventional approaches. The magnetoelectric effect is

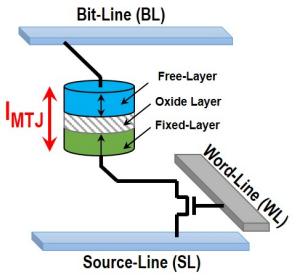


Fig. 2: 1T-1R STT-MRAM cell structure.

achieved via utilizing an electric field in order to change the state of the magnetic devices such as MTJs. Using the magnetoelectric effect, MTJ devices will benefit from *faster and more efficient switching while consuming less energy* [14–16]. Recent research studies have shown that use of the VCMA effect facilitates the use of an electric field to ease or eliminate the demand of charge current for switching the state of MTJ devices. VCMA generates an electric field that causes an accumulation of electron charge and results in a change of occupation of atomic orbitals at the interface, which causes a change in the magnetic anisotropy of the MTJ. Using a VCMA approach can result in a deterministic change of the magnetic state of the MTJ in an *energy-efficient* and *rapid* manner. In other words, use of VCMA can lower the energy barrier between the P and AP states and facilitate the MTJ to switch states using a voltage applied across its terminals. The effective Perpendicular Magnetic Anisotropy (PMA) of an MTJ in the presence of VCMA effect can be modeled using the following equations [14]:

$$K_{eff}(V_b) = \frac{M_s H_{eff}(V_b)}{2} = \frac{K_i(0) - K_i(V_b)}{t_f} - 2\pi M_s^2, \quad (1)$$

$$\Delta(V_b) = \frac{E_b(V_b)}{k_B T} = \Delta(0) - K_i(V_b)\frac{A}{k_B T}, \quad (2)$$

$$V_c = \Delta(0)\frac{k_B T t_{ox}}{A\xi}, \quad (3)$$

where V_b is the bias voltage applied via VCMA effect, $K_{eff}(V_b)$ is the effective PMA, $H_{eff}(V_b)$ is the effective magnetic field in the presence of bias voltage, M_s is the saturation magnetization, $K_i(0)$ is the initial interfacial PMA energy, $K_i(V_b)$ is the interfacial PMA energy after applying the bias voltage, t_f is the MTJ's free-layer thickness, A is the sectional area of the MTJ, $\Delta(0)$ is the thermal stability factor under zero bias voltage, $\Delta(V_b)$ is the thermal stability factor under bias voltage of V_b, $E_b(V_b)$ is the voltage-dependent energy barrier, k_B is the Boltzmann constant, T is the temperature, V_c is the critical voltage required by VCMA effect to modify the energy barrier, ξ is the VCMA coefficient, and t_{ox} is the MTJ's oxide thickness.

VCMA-MTJ devices require a bias voltage to lower their energy barrier between the two stable states of Parallel (P) and Anti-Parallel (AP). This will result in a more efficient method of switching the device between the P and AP states. When the energy barrier is lowered, a current with smaller magnitude and pulse duration can switch the magnetic orientation or the state of the MTJ devices. As a result, the energy consumption of the write operation will be reduced. The VCMA bias voltage that is required to modify the energy barrier can be found using (3). Additionally, as experimental results in [14–16] have shown, $K_i(V_b)$ demonstrates a linear dependency to the electric field, hence, we can simplify it as $K_i(V_b) = \xi\frac{V_b}{t_{ox}}$ [14].

Furthermore, modeling of the VCMA effect can be realized through modifying the Landau-Lifshitz-Gilbert (LLG) equation, shown in (4), while updating $\vec{H_{eff}}(V_b)$. As shown in (6), the voltage dependent anisotropy field, $\vec{H_{ani}}(V_b)$, changes with the VCMA bias voltage. The changes in (6) will then result in the modification of $\vec{H_{eff}}(V_b)$ in (5), which presents the effective magnetic field vector. As a result, the VCMA effect will enable the MTJ devices to switch faster and with reduced switching currents due to the lowered energy barrier caused by the VCMA bias voltage. By requiring reduced current magnitude for a shorter pulse duration, this approach will reduce the overall energy consumption of MTJ devices during the write operation. Additionally, in order to observe the switching of the magnetic orientation of the MTJ devices in the z-axis of the Cartesian coordinate system, we need to solve the LLG equation shown in (4). The modifications made in the LLG equation to model the VCMA effect are shown below [14]:

$$\frac{\mathrm{d}\vec{m}}{\mathrm{d}t} = -\gamma\vec{m}\times\vec{H}_{eff}(V_b) + \alpha\vec{m}\times\frac{\mathrm{d}\vec{m}}{\mathrm{d}t} - \rho_{stt}\vec{m}\times(\vec{m}\times\vec{m}_r), \quad (4)$$

$$\vec{H}_{eff}(V_b) = \vec{H}_{ext} + \vec{H}_{dem} + \vec{H}_{th} + \vec{H}_{ani}(V_b), \quad (5)$$

$$\vec{H}_{ani}(V_b) = \left(\frac{2K_i(0)t_{ox} - 2\xi V_b}{\mu_0 t_f M_s t_{ox}}\right)m_z, \quad (6)$$

where $\vec{m}$ is the magnetization vector of the MTJ's free-layer $\{m_x, m_y, m_z\}$, $\vec{m}_r$ is the polarization vector, γ is the gyromagnetic ratio, α is the Gilbert damping factor, $\vec{H}_{eff}(V_b)$ is the effective magnetic field vector in the presence of bias voltage, ρ_{stt} is the STT factor, $\hbar$ is the reduced Planck constant, P is the STT polarization factor, J_{stt} is the driving current density inducing STT, e is the elementary electron charge, μ_0 is the vacuum permeability, $\vec{H}_{ext}$ is the external magnetic field vector $\{H_x, H_y, H_z\}$, $\vec{H}_{dem}$ is the demagnetization field vector, $\vec{H}_{th}$ is the thermal noise field vector, and $\vec{H}_{ani}(V_b)$ is the voltage-dependent anisotropy field vector. As it can be observed from (6), using the VCMA effect, by applying a positive bias voltage across the MTJ, the PMA will be reduced and will result in reduction of its coercivity. On the other hand, by applying a negative voltage across the MTJ, the PMA will be increased and as a result, its coercivity will increase as well. Fig. 3 shows the effects of VCMA on an MTJ device.

C. Proposed AIQ Architecture

In recent studies, researchers have exploited the use of emerging devices for signal processing applications. In particular, they have explored designing ADCs using emerging devices such as SHE-MTJ [20], Domain Wall Motion (DWM) [23], and Racetrack Memory [29]. Herein, we propose

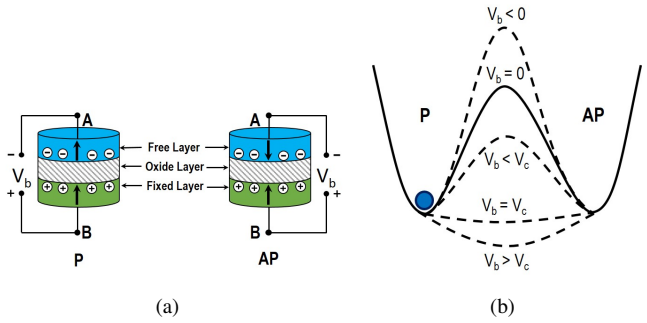


Fig. 3: (a) Structure of the VCMA-MTJ. (b) Modification of energy barrier ($E_b(V_b)$) using the VCMA effect. When $V_b > V_c$, the energy barrier is completely eliminated. Additionally, if $0 < V_b < V_c$, the energy barrier will be reduced to facilitate the switching of the state of the MTJ. On the other hand, for $V_b < 0$ the energy barrier will increase.

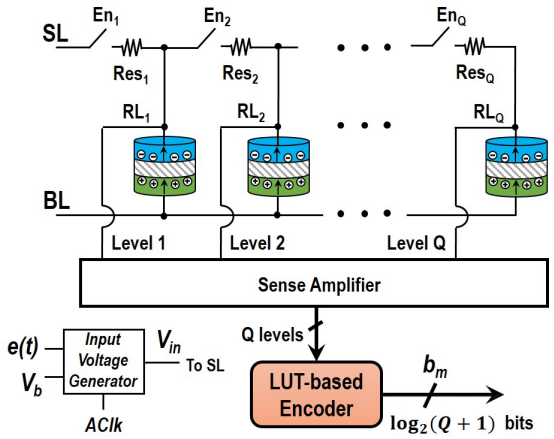


Fig. 4: The Proposed AIQ Architecture.

an *Adaptive Intermittent Quantizer (AIQ)* to perform signal sampling and quantization. AIQ uses VCMA-MTJ devices to provide fast SR and adaptive QR, along with energy-efficient sampling and quantization operations. Use of VCMA-MTJs enables AIQ to provide various quantization levels by changing the energy barrier of MTJ devices. An example of Q-level AIQ architecture is shown in Fig. 4, where Q is the number of QR levels determined by the optimization algorithm described in Section IV. The operation of AIQ has three main steps:

- First, during the Reset step, all active VCMA-MTJ devices will be reset to zero representing a Parallel state,
- Second, during the Sampling step, based on the determined SR and QR (as discussed in Section IV-D), first a bias voltage, V_b, will be applied across the active VCMA-MTJ devices' terminals to modify and set their energy barrier followed by the analog input, $e(t)$, to write into the active VCMA-MTJ devices, as shown in Fig. 1(a), and
- Third and final step is the Read (or Sensing) step to sense the data stored in each device using a sense amplifier in a conventional fashion.

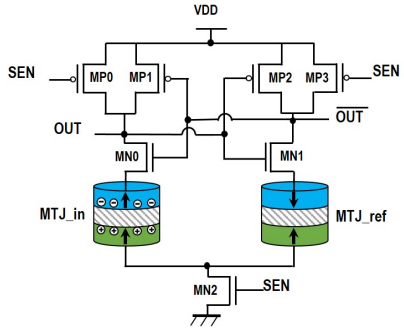


Fig. 5: Schematic of the PCSA used to read the state of an MTJ.

Based on the architecture shown in Fig. 4, during the Reset step, Source Line (SL) is set to zero, Bit Line (BL) is set to one, and Read Lines (RLs) are high impedance, which causes all devices to go to the P state. During the Sampling step, SL is set to input voltage (V_{in}), BL is set to zero, and RLs are high impedance. In this state, an Input Voltage Generator circuit is used to allow the VCMA bias voltage, V_b, followed by the analog input, $e(t)$, to be applied through V_{in} to adjust the threshold of MTJ devices and write into the MTJs. A signal called Adaptive Clock (AClk), which is set based on the $\tau^{(n_f)}$ as described in Section II, will control the sampling rate of the input signal. During the Read (or Sensing) step, SL is set to high impedance, BL is set to zero, and RLs are sent to sense amplifiers to read the value stored in each MTJ. The design of the sense amplifiers for an MTJ read operation is discussed broadly in the literature [12].

The combination of switches and resistors included in our proposed architecture is used to realize the *adaptive quantization resolution levels*. The switch ladder is used to adaptively set the resolution and the resistance ladder is used to provide different VCMA bias voltages, V_b, for different MTJs. By providing different bias voltage levels for different MTJs, some MTJs turn on with lower input voltages while some require higher input voltages to switch state. Furthermore, the switches, which are realized using transmission gates in order to provide reliable switching [11], enable the Adaptive SR/QR Controller shown in Fig. 1(a) to optimize the QR by turning unused MTJs off. As demonstrated subsequently, this results in significant energy savings.

As shown in Fig. 5, a Pre-Charge Sense Amplifier (PCSA) [24] is used to read the value stored in the SHE-MTJ devices. In the PCSA, during the pre-charge stage, **SEN** signal is low, turning MN2 off while turning MP0 and MP3 on. This will pre-charge the output nodes **OUT** and $\overline{\textbf{OUT}}$ to **VDD**. As a result, MN0 and MN1 will turn on while MP1 and MP2 are still off. As soon as the sensing stage begins, MP0 and MP3 turn off and MN2 turns on. As a result, based on the difference between **MTJ_In** and **MTJ_ref** resistances, which is determined by the magnetization orientation of their free-layer compared to their fixed-layer, one of the two output nodes begins to discharge more rapidly to **GND**, leading either MP1 or MP2 to turn on and charge the other output to **VDD**.

The AIQ circuit provides different QR levels. A Look-up

Table (LUT)-based encoder is used to encode the values for different levels into bits. For instance, the example shown in Fig. 4 can provide 1 bit with 1 level, 2 bits with 3 levels, 3 bits with 7 levels, and so forth. Since the number of active components of the LUT-based encoder depends on the number of active levels, spin-based devices have also been utilized within the encoder structure. Correspondingly, depending on how many QR levels our algorithm is using, we can adaptively disable the parts of the LUT-based encoder that are not being used in the encoding process. This will lead to significant energy savings and improved performance as shown in [13] compared to conventional CMOS encoders since spin-based devices offer zero leakage energy consumption.

The behavior of a single VCMA-MTJ device is demonstrated in Fig. 3. As it is observed different values of V_b results in different energy barrier heights. As discussed earlier in this Section, different energy barrier heights result in different switching behavior for the VCMA-MTJ devices. In our proposed AIQ design, we have utilized an example of 255 VCMA-MTJ devices to realize a wide range of quantization resolutions from 1-bit to 8-bit ADC operation. Additionally, different V_b values will be applied to the active VCMA-MTJ devices to realize discriminable quantization resolutions. Moreover, for 1-bit resolution, one level is used, which is set to 650mV and in the middle of our signal range that is normalized between $[0 - 1.3]$V. Additionally, the levels are spaced by 542mV, 201mV, 90mV, 43mV, 21mV, 10mV, and 5mV for 2-bit, 3-bit, 4-bit, 5-bit, 6-bit, 7-bit, and 8-bit resolution levels, respectively.

IV. Energy-Aware Quantized CS via Adaptive Rate and Resolution

A. Background and Related Work

The proposed architecture utilizes tools from the general theory of Compressive Sensing (CS) [9, 10] and hardware-specific constraints to minimize the overall cost of acquisition for wide-band but spectrally sparse signals. Spectrally sparse signals arise in many applications such as cognitive radio networks, frequency hopping communications, radar/sonar imaging systems, and musical audio signals. In many cases, the sparse components are spread over a wide-band spectrum and need to be acquired without prior knowledge of their frequencies. This is a major challenge in spectrum sensing that is an essential block in any spectrum-aware communication system. Spectrum-aware communication networks require Radio Frequency (RF) and mixed-signal hardware architectures that can achieve very wide-band but energy-efficient spectrum sensing.

Several architectures have already been proposed for wide-band signal acquisition at rates close to its information rate. These include the Random Demodulator (RD) [30–32], the Multi-coset Sampler [33] and the Modulated Wideband Converter (MWC) [34, 35]. However, the measurements need to be quantized and encoded to bits for subsequent transmission or processing. In many potential applications the available bit budget is constrained, which suggests a trade-off between the SR and QR. This trade-off is well studied in the Quantized Compressive Sensing [25–28] literature. Generally speaking, in high observation SNR, fewer but fine-quantized measurements yield better reconstruction quality. However, in the low SNR case, more but coarse-quantized measurements are preferred. As the observation noise varies during acquisition, dynamic optimization of the rate/resolution trade-off is favorable, which is a key innovation of our approach.

So far, several algorithms have been proposed for sparse signal reconstruction from quantized measurements [36, 37]. The extreme case of 1-bit compressive sensing has been extensively studied [38–41]. In the proposed architecture, the input signal is compared with the level signal, and measurements of the error are acquired. The level signal is adaptively predicted in a feedback loop at the ADC. The idea of acquiring sign measurements of level comparisons was applied in [42] to overcome the scale ambiguity in 1-bit CS reconstruction. In [43, 44], the levels were adaptively varied during acquisition.

The proposed architecture considers both the reconstruction-level and hardware-level cost functions to adapt and optimize the instantaneous sampling rate and quantization resolution along acquisition. The reconstruction-level cost originates from the constrained bit budget as mentioned above, and the hardware-level cost is the power consumed by the underlying hardware for sampling and quantization.

There has been some effort to investigate the trade-off between resolution and the rate in a sensing system [28, 45–47]. However, most of the related works do not include the power constraint in their model. For instance, as in [45], Fisher information can be used to quantize the asymptotic performance of the sensing system. More related to the developed scheme, authors in [28] derived an upper bound for error of quantized compressive sensing without any power constraints. Most recently, authors in [47] derived Cramer-Rao bound for quantized compressed sensing and investigated the trade-off between SR and QR. However, to the best of our knowledge, there is no work on investigating the rate/resolution trade-off under both power and bandwidth constraints for quantized compressive sampling systems.

B. Spectrally-Sparse Signal Model

Similar to [30–32, 48], we approximate a spectrally sparse signal $x(t)$ by the sum of exponential components $x(t) = \sum_{s\in S} x_s(t)$ in which $S = \{s_1, s_2, ..., s_N\}$ and $x_{s_i}(t+\epsilon) = e^{s_i\epsilon}x_{s_i}(t)$ and assume that only a few number of the components have significant amplitudes $\|x_s(t)\|_0$.

Now consider a frame of the signal as $X_m = \begin{bmatrix} x(m\tau) & x((m-1)\tau) & \cdots & x((m-M+1)\tau) \end{bmatrix}^T$ in which ($\tau = \tau^{(n_f)}$) is the corresponding sample period adapted for the frame and $T = (M-1)\tau$ is the frame length. Let us define Φ by

$$\Phi = \begin{pmatrix} 1 & 1 & \cdots & 1 \\ e^{-s_1\tau} & e^{-s_2\tau} & \cdots & e^{-s_N\tau} \\ \vdots & \vdots & \ddots & \vdots \\ e^{-s_1(M-1)\tau} & e^{-s_2(M-1)\tau} & \cdots & e^{-s_N(M-1)\tau} \end{pmatrix}. \tag{7}$$

We can write $X_m = \Phi X'_m$, where $X'_m = \begin{bmatrix} x_{s_1}(m\tau) & x_{s_2}(m\tau) & \cdots & x_{s_N}(m\tau) \end{bmatrix}^T$ is the sparse representation of X_m. Defining a diagonal predictor matrix $P = Diag(e^{Ms_1\tau}, e^{Ms_2\tau}, \cdots, e^{Ms_N\tau})$, we get $X'_m = PX'_{m-M}$, which shows the relation between the sparse representations of the signal for two consecutive frames. This relation later will help us in designing an iterative reconstruction algorithm.

C. Sparse Component Estimation (SCE)

Consider the signal model addressed in IV-B. Moreover, let a frame of the corresponding estimate signal $l(t)$ and the corresponding quantized symbols c_m's be denoted by $L_m = \begin{bmatrix} l(m\tau) & l((m-1)\tau) & \cdots & l((m-M+1)\tau) \end{bmatrix}^T$ and $C_m = \begin{bmatrix} c_m & c_{m-1} & \cdots & c_{m-M+1} \end{bmatrix}^T$, respectively. We can formulate the sparse spectral estimation as

$$\hat{X'_m} = \arg\min_{X'_m} \|X'_m\|_0 \qquad s.t. \quad C_m = AQ(\Phi X'_m - L_m), \tag{8}$$

in which $AQ(.)$ is the element-wise *Adaptive Quantizer* operator. The number of quantization levels is a function of the optimized QR values, and it changes adaptively during acquisition.

To estimate the vector of sparse components X'_m, we take an iterative gradient-based optimization approach followed by hard thresholding similar to [36]. To this end, we solve (9), in which the first term of the cost function enforces consistency with the sequence of quantized symbols, the second term guarantees smooth update of the solution, and the constraint ensures sparsity of the solution. Note that in (9), $\hat{X'}_{m-M}$ represents the estimate of the vector of sparse components for the previous frame and K is the number of non-zero spectral components.

$$\begin{aligned} \hat{X'}_m = \arg\min_{X'_m} \; & \|C_m - AQ(\Phi X'_m - L_m)\|_2^2 \\ & + \lambda \left\| X'_m - P\hat{X'}_{m-M} \right\|_2^2 \quad s.t. \quad \|X'_m\|_0 \le K \end{aligned} \tag{9}$$

To decrease the computational complexity, we take a sliding window strategy and apply only one iteration of gradient descent on each frame utilizing the estimate of the previous frame as an initial estimate. This is different from the literature on Quantized Compressive Sensing (QCS) which propose reconstruction algorithms that are both iterative and batch-based. This means that the previously proposed reconstruction algorithms need to apply several iterations on each frame of the input signal to reconstruct the sparse spectral components. Thus, such is not only computationally demanding, but also introduces a frame processing delay at least equal to the frame length. Utilizing the sliding window approach decreases the computational burden and enables the proposed algorithm to dynamically follow slow changes in the input signal along iterations.

D. Adaptive Energy-Aware SR/QR Optimization

For a clear exposition of our rationale, we assume that the frame length is adjusted such that the signal and noise statistics do not change significantly during a single frame. As a result, there exists a single QR and SR that optimizes the performance metric for that frame. However, the optimal SR and QR might change from frame to frame. We further assume that the frame length is fixed during signal acquisition. Thus, to optimize the SR, we need to optimize the number of measurements M per frame.

To formalize the SR/QR optimization problem, consider a bandwidth constraint that enforces the total number of acquired bits to be less than a bit budget, i.e., $M^{(n_f)}\beta^{(n_f)} \le \mathcal{B}^{(n_f)}$, where $M^{(n_f)}$ is the number of measurements, $\beta^{(n_f)}$ is the bit resolution of the measurements, and $\mathcal{B}^{(n_f)}$ is the bit-budget for frame n_f. Furthermore, the energy constraint can be expressed as $\mathcal{E}(\beta^{(n_f)}, M^{(n_f)}) < C_p^{(n_f)}$, where $\mathcal{E}(\beta, M)$ is the required sensing energy as function of SR and QR and $C_p^{(n_f)}$ is the energy available to the device for sampling the frame n_f. Based on the discussion presented in Section V-A, an estimation for the dynamic energy consumption of the proposed architecture is $\mathcal{E}(\beta, M) = 16.63 \times 2^{\beta} M$ (fJ/frame). To find the optimal values of β and M at each frame, i.e. $\beta^{(n_f)}$ and $M^{(n_f)}$, we need to solve the following problem:

$$\begin{aligned} \text{minimize} \quad & F^{(n_f)}(M, \beta), \\ \text{subject to} \quad & M\beta \le \mathcal{B}^{(n_f)}, \\ & \mathcal{E}(\beta, M) < C_p^{(n_f)}. \end{aligned} \tag{10}$$

$F^{(n_f)}(M, \beta)$ is the error metric at frame n_f. In general, the reconstruction performance can be a function of signal characteristics such as SNR and sparsity level, leading to potentially different error metric $F^{(n_f)}(M, \beta)$ for different frames.

In this work, we use the upper bound of the reconstruction error as the error metric, due to its popularity in CS literature. Assume that the signal being sampled at frame n_f can be represented in terms of only K bases out of the N available bases and the nonzero coefficients are drawn from a zero-mean Gaussian with standard deviation $\sigma_x^{(n_f)}$. Further, the signal is contaminated with zero-mean Gaussian noise with standard deviation $\sigma_n^{(n_f)}$. Due to [28], we can approximate the upper bound on reconstruction error as:

$$\frac{c}{M\beta}(K{\sigma_x^{(n_f)}}^2 \beta 2^{(-2\beta)} + N{\sigma_n^{(n_f)}}^2 \beta(1 + 2^{(-2\beta)})), \tag{11}$$

where c is a constant and the signal parameters, i.e., $\sigma_n^{(n_f)}$ and $\sigma_x^{(n_f)}$, can be estimated from previous time frames. Thus, we can use the expression in (11) as the objective of the optimization problem formulated in (10). The result of optimizing this problem is used as a lookup table in the proposed acquisition scheme to adapt the optimal SR and QR values in an online manner during acquisition. Optimization results considering the power and bandwidth constraints are reported in Section V-B, which gives us intuition into the inner workings of the SR/QR trade-off.

V. Simulation Results and Analysis

A. AIQ Sampling Results and Performance Analysis

In order to evaluate and validate the behavior and functionality of the proposed AIQ design, SPICE and MATLAB simulations were performed. We have utilized the 22nm Predictive Technology Model (PTM) [49] as well as VCMA-MTJ model represented in [14] along with other circuit parameters and constants listed in Table I in our simulations to implement and evaluate the proposed AIQ design.

To examine the performance and potential of the VCMA-MTJ devices in circuit designs and applications, the circuit behavior of VCMA-MTJ devices maintaining resistance in P ($\theta = 0°$) and AP ($\theta = 180°$) states as well as the voltage-dependent TMR effect are modeled by Kang, et al. [14] and expressed using the following equations [11, 14]:

$$R_P = \frac{t_{ox}}{Factor \times Area \cdot \sqrt{\phi}} \exp\left(\frac{2\sqrt{2me}}{\hbar} \times t_{ox} \cdot \sqrt{\phi}\right) \tag{12}$$

$$TMR(V_b) = \frac{TMR(0)}{1 + (\frac{V_b}{V_h})^2} \tag{13}$$

$$R_{MTJ}(V_b) = R_P \frac{1 + (\frac{V_b}{V_h})^2 + TMR(0)}{1 + (\frac{V_b}{V_h})^2 + TMR(0)[0.5(1 + \cos(\theta))]} \tag{14}$$

where V_b is the bias voltage, $TMR(V_b)$ is the Tunnel Magneto-Resistance (TMR) ratio, $V_h = 0.5V$ is the bias voltage when TMR ratio is half of the $TMR(0)$, t_{ox} is the oxide thickness of MTJ, $Factor$ is obtained from the resistance-area product value of the MTJ that relies on the material composition of its layers, $Area$ is the surface area of the MTJ, and ϕ is the oxide layer energy barrier height. The switching of the perpendicular magnetization of the VCMA-MTJ's free-layer is determined by θ is the polar angle of the magnetization vector of the free-layer, $\vec{m}$. In other words, $m_z = cos(\theta)$ provides the component of the magnetization vector, $\vec{m}$, along the z-axis of the Cartesian coordinate system. The parameters and constants used in the VCMA-MTJ model for the simulation results are provided in Table I [14].

As depicted in Fig. 6(b), a growing sinusoidal signal is sampled by 3 levels to 2 bits based on the AClk signal, shown in Fig.6(a), with 12 sampling intervals resulting in the bit budget of $\mathcal{B}^{(n_f)} = 24$. Additionally, Fig. 6(c) illustrates the switching of each of the 3 VCMA-MTJ devices with different switching energy barriers resulting in different levels. According to our results, the energy consumption of this sampling configuration equals 596.31fJ, which consists of the reset, sample, and read operations as well as the peripheral circuitry energy consumption during the 50ns signal duration. The corresponding quantized CS reconstruction algorithm achieves a Mean Square Error (MSE) of 4.7×10^{-5} on this signal which proves efficient reconstruction capability of the proposed design. Furthermore, Fig. 7(b) depicts sampling of the same growing sinusoidal using the AClk signal with 8 sampling intervals, as shown in Fig. 7(a), to achieve to 3 bits resolution while maintaining the same bit budget of $\mathcal{B}^{(n_f)} = 24$. Moreover, Fig. 7(c) demonstrates the switching of each of the 7 VCMA-MTJ devices. The energy consumption of this configuration is 906.39fJ during the 50ns signal duration. The proposed reconstruction algorithm achieves an MSE of 1.2×10^{-4} in this case.

TABLE I: Circuit parameters and constants with their corresponding values for the VCMA-MTJ model.

Parameter	Description	Default Value
M_s	Saturation magnetization	$0.625 \times 10^6 A/m$
$K_i(0)$	Initial interfacial PMA energy	$0.32 mJ/m^2$
t_f	Free-layer thickness	$1.1nm$
α	Gilbert damping factor	0.05
$\Delta(0)$	Thermal stability factor at $V_b = 0$	40
T	Temperature	$300K$
ξ	VCMA coefficient	$60 fJ/V \cdot m$
t_{ox}	Oxide-layer thickness	$1.4nm$
H_x	External Magnetic Field	4.8×10^4 °$/m$
P	STT polarization factor	0.58
d	MTJ diameter	$50nm$
ϕ	Potential barrier of MgO	$0.4V$
$TMR(0)$	TMR ratio at $V_b = 0$	200%
V_h	Bias Voltage at TMR2	$0.5V$
Constants	**Description**	**Default Value**
γ	Gyromagnetic ratio	$2.21276 \times 10^5 m/(A \cdot s)$
k_B	Boltzmann constant	$1.38 \times 10^{-23} J/K$
μ_0	Vacuum permeability	$1.2566 \times 10^{-6} H/m$
m	Electron mass	$9.11 \times 10^{-31} kg$
e	Elementary charge	$1.6 \times 10^{-19} C$
$\hbar$	Reduced Planck constant	$1.054 \times 10^{34} Js$

It is observed that as the bit budget is fixed in the experimental scenarios of Fig. 6 and Fig. 7, an increase in the number of QR results in a decreased SR considering the SR / QR trade-off introduced in Section IV-D. This is observed in Fig. 6(b) and Fig. 7(b) when the number of samples is decreased from 12 to 8 in the provided snapshot of the signal. The MSE values achieved show that for the experiment parameters (noise, power, bit budget, etc.), an increased number of coarsely quantized samples, as shown in Fig. 6, perform better than accurately quantized samples acquired at a decreased rate, as shown in Fig. 7.

According to our results, the energy consumption of each VCMA device is $\sim$ 17fJ, which consists of a reset and a sample operation for a single VCMA-MTJ device. Meanwhile, the energy consumption of the peripheral circuit that sets the VCMA bias voltages and performs the read operation is $\sim$ 2fJ. Fig. 8 illustrates the energy consumption versus QR for 22nm technology node, considering two different sampling rates of 5 samples and 10 samples within the same sampling duration of 50ns. It can be observed that for every extra resolution bit, the number of VCMA-MTJs added to the design to provide required QR levels grows exponentially. As a result, the number of reset, sample, and read operations will increase based on the number of active levels. It is known that the lower bound for power of ADCs grows exponentially for every bit of resolution [50, 51]. Thus, QR plays a crucial role in the energy cost of the device. The energy consumed by the proposed MTJ devices can be simplified to a formula to calculate and estimate the amount of dynamic energy consumption for each frame as $E_L \times 2^\beta M$, where E_L is the dynamic energy per QR level that is a technology dependent value. According to our simulation results, the E_L value equals 16.63fJ. Hence, the energy per frame is given by $16.63 \times 2^\beta M$, where β is the number of bits and M is the number of samples.

Accordingly, for every VCMA-MTJ read, write, and reset

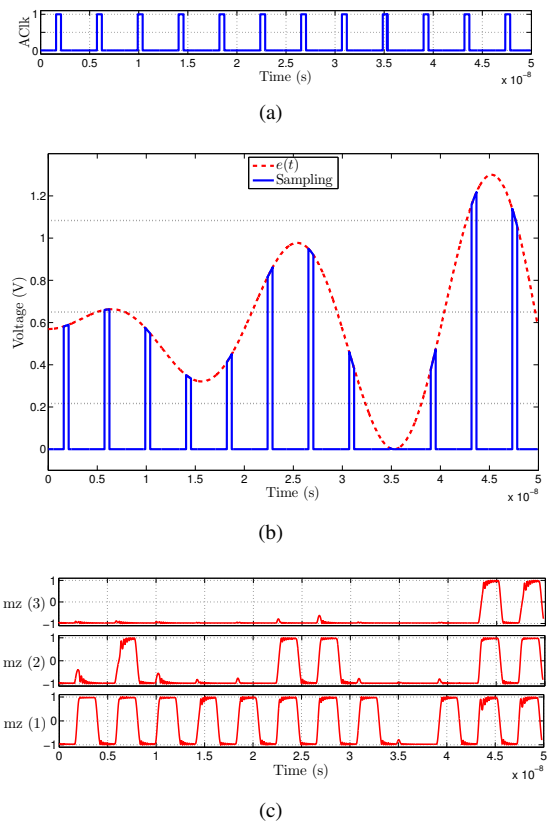


Fig. 6: (a) shows the AClk signal over time, (b) depicts the $e(t)$ signal being sampled with 2 bits (3 levels) with 12 sampling intervals, and (c) illustrates the switching of the 3 VCMA-MTJ devices in the sampling intervals.

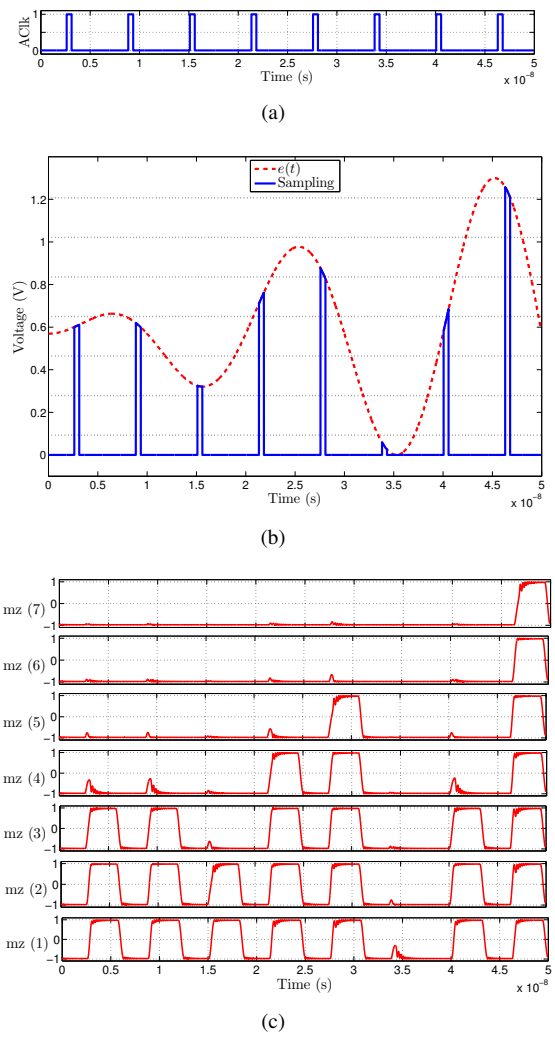


Fig. 7: (a) shows the AClk signal over time, (b) depicts the $e(t)$ signal being sampled with 3 bits (7 levels) with 8 sampling intervals, and (c) illustrates the switching of the 7 VCMA-MTJ devices in the sampling intervals.

operations, approximately 16fJ is required using a 22nm technology node library. The aforementioned energy equation can be employed in the SR/QR optimization process as discussed in Section IV-D. According to our results, it can be estimated that using VCMA-MTJ devices, overall reset, sample, and read operations would require about 1ns in 22nm technology node library to provide a reliable outcome. As the results show, increasing the QR can increase the energy consumption due to the increase in the number of active MTJ devices. However, by decreasing SR if possible, in cases where increased QRs are required, energy consumption can be decreased. Additionally, an increase in the SR can result in an increase in the energy consumption of AIQ. This is because an increase in SR requires fast reset, sampling, and read steps. Hence, the MTJ devices require to be demagnetized at a faster pace, which can incur extra energy cost. This would be exacerbated if an increase in QR is required, since additional devices will need to be rapidly demagnetized. Overall, energy consumption in the hardware is not simply a function of the bit budget, i.e., $\mathcal{B}^{(n_f)}$. Rather, it is a complex function of its components SR and QR as well as circuit elements and peripherals that are added for every additional quantization level. In this paper, we investigated and formulated the hardware energy cost and trade-offs as a function of SR and QR and utilized the results in the proposed cross-layer energy-aware SR/QR optimization, as discussed in Section IV-D.

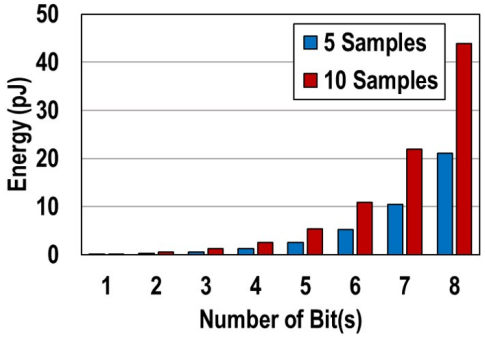


Fig. 8: Energy consumption versus Quantization Resolution (QR).

B. SR and QR Optimization

Fig. 9 shows the values of SR and QR that minimize the upper bound in (11). As shown, for low SNRs (< 10 dB), the device needs to sample more measurements with QR of only 1 bit. This is intuitive, since capturing a low quality signal

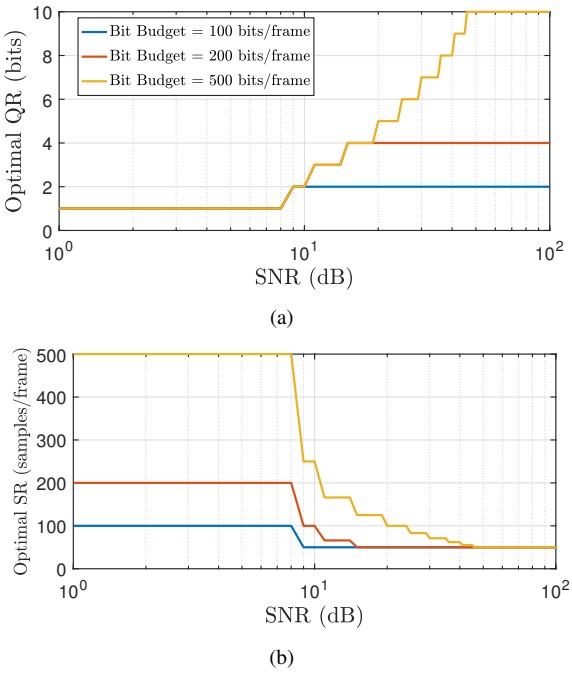


Fig. 9: Optimal values of SR and QR for different SNRs for signal dimension of $N = 1000$ and and sparsity level of $K = 50$, without considering the energy constraints.

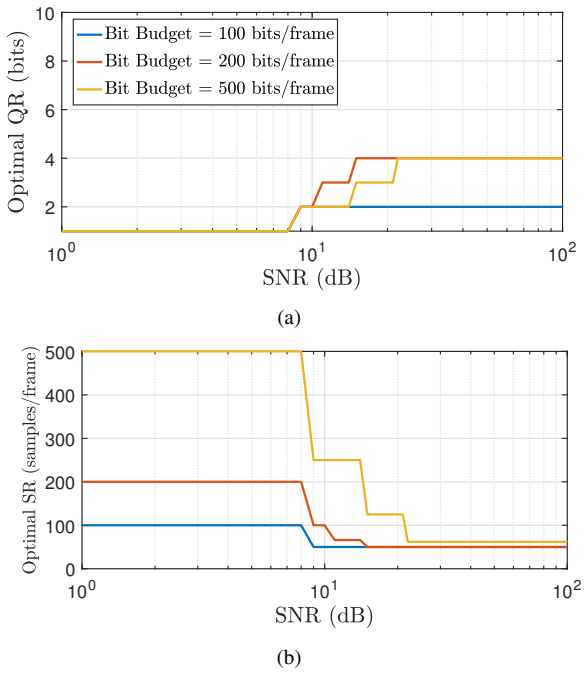


Fig. 10: Optimal values of SR and QR for different SNRs. The dynamic energy of AIQ is constrained to be less than 17.03pJ/frame. $N = 1000$ and $K = 50$.

with high-resolution is wasteful. As the SNR increases, the optimal QR increases and the device should sample the signal with fewer high resolution measurements. For instance, for a bit budget of 500 bits and SNR of 50 dB, we should collect only 50 samples with 10 bits of resolution. These results, and other similar works in the literature [45, 47, 52], ignore the energy cost of the sensing task.

To investigate the energy-aware SR/QR optimization, Fig. 10 shows optimal QR and SR for the case when the energy cost of sampling is taken into account. In this simulation, it is assumed that the dynamic energy budget for AIQ is 17.03 pJ/frame. As expected, the energy constraint changes the outcome of the SR/QR optimization. For instance, for a bit budget of 500 bits and in a high SNR regime, the device is limited by the power constraint and is not able to collect high resolution samples.

Furthermore, to illustrate the necessity of adapting SR and QR during acquisition, we plot the optimal QR and SR values versus the frame number in Fig. 11. Note that in this simulation scenario, the variance for the $e(t)$, which is the input to our proposed AIQ block, is decreasing with the frame number. This is because $l(t)$ becomes increasingly accurate estimate of $x(t)$ along iterations. However, the input noise is considered random. The resulting SNR along with the QR and SR values that minimize the performance upper bound and the energy bound introduced in Section IV-D are provided in Fig. 11. As the SNR of the signal varies over time, the controller needs to tune the SR and QR to minimize the error metric. It is also worthwhile to point out the fact that, due to exponential growth of the energy with QR, the energy constraint prevents us from sampling the signal with high QR. Thus, adding an energy budget to the simulation places a limit on the QR. These results further encourage adaptive and energy-aware adjustments of SR and QR to improve the performance of the proposed signal acquisition process.

Fig. 12 shows the reconstruction results for 10 consecutive frames of a sparse signal generated at random with 5% spectral sparsity factor. The signal is sampled non-uniformly in frames of 2.5×10^{-2} seconds. In this simulation, the bit budget is 25 bits/frame and the energy budget is 850 fJ/frame. Fig. 12(a) shows the input and level signals, i.e., $x(t)$ and $l(t)$. Fig. 12(b) shows the optimal SR and QR values derived from signal statistics and, Fig. 12(c) shows the corresponding error signal $e(t)$, which is normalized in $[0 - 1.3]$V to reside in the input operation range of the AIQ circuit. Additionally, Fig. 12(c) depicts the optimized non-uniform sampling instances utilizing the proposed AIQ circuit.

C. Reliability Analysis

In order to evaluate the functionality of our proposed AIQ design in the presence of Process Variation (PV), we have conducted a series of Monte Carlo (MC) simulations with $10,000$ instances for the sample operation and $10,000$ instances for the read operation. During the MC simulation, we have considered 10% variation for the components of the peripheral circuitry such as threshold voltage of the CMOS transistors as well as 1% variation for the MTJ devices in agreement with [53]. This can cover a wide range of possible variations enabling a comprehensive PV analysis. We have analyzed our circuit separately for sample operation, as well as read operation. The results of the reliability analysis for the sample operation are shown in Fig. 13. As it can be observed

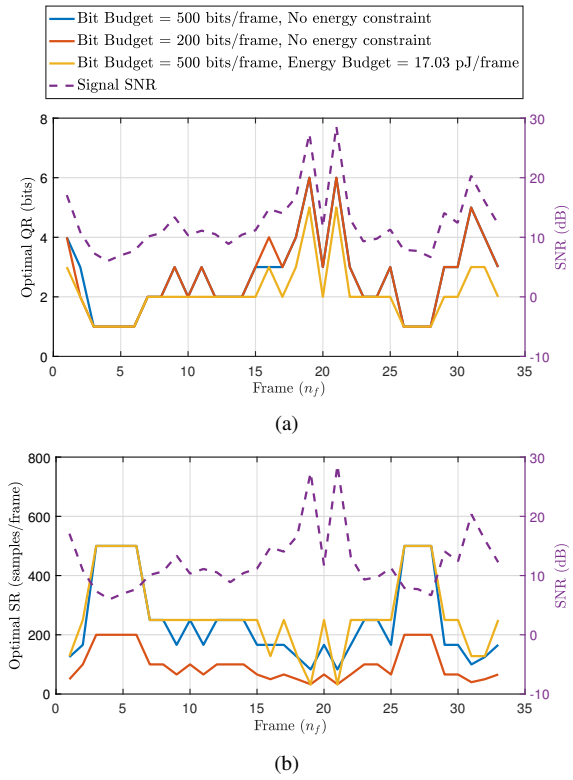


Fig. 11: (a) Optimal QR and (b) optimal SR for different frames. The dashed line shows the SNR of the signal.

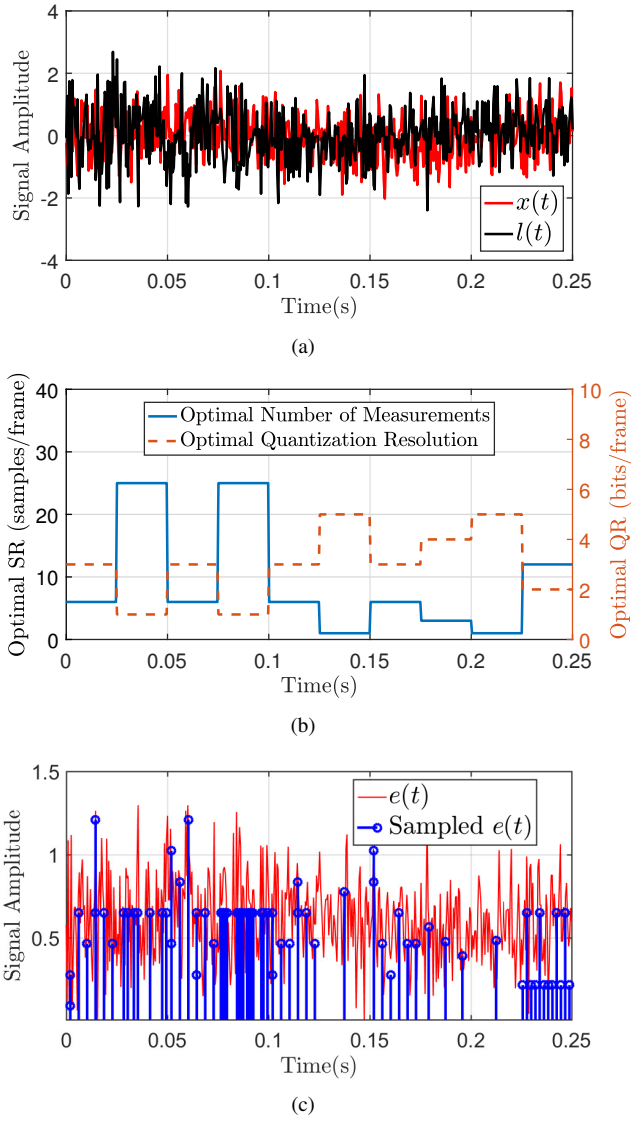


Fig. 12: The reconstruction results for a typical sparse signal sampled by the proposed scheme.

from Fig. 13(a), for sampling duration within the range of 3ns to 3.5ns with VCMA-MTJ switching duration within the range of 0.4ns to 0.5ns, depicted as dark blue region in Fig. 13(a), the sample error rate is near 0.0%. However, in order to minimize the energy consumption of the sample operation, sample duration should be within the range of 5ns to 5.5ns with VCMA-MTJ switching duration within the range of 0.3ns to 0.35ns according to Fig. 13(b). Hence, there is a trade-off between sample error rate and energy consumption. Thus, the dark blue region in Fig. 13(b) reflects a reduced energy consumption at the expense of the corresponding sample error rate indicated in Fig. 13(a).

Furthermore, the results of the reliability of the read circuit are provided on Fig. 14. Herein, we have conducted the reliability analysis for the four of the most commonly-used approaches for sensing according to the study presented in [53]. As shown in Fig. 14, the Variation Immune Sense Amplifier (VISA) proposed in [11] and the Separated Pre-Charge Sense Amplifier (SPCSA) proposed in [54], provide highly-reliable outputs considering Tunnel Magnetoresistance Ratio (TMR) of 200% by only incurring 0.05% and 0.07% error rate during the read operation, respectively. However, VISA and SPCSA incur large area and energy consumption overheads compared to the Energy Aware Sense Amplifier (EASA) proposed in [11] and the Pre-Charge Sense Amplifier (PCSA) proposed in [24]. As shown in [53], EASA and PCSA provide area- and energy-efficient sensing circuits, while VISA and SPCSA provide more reliable sensing circuits at the cost of increased energy consumption and area footprint.

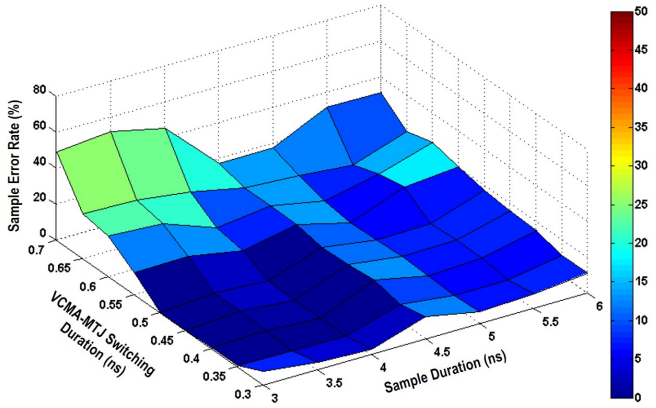
D. Comparisons

In Table II, we compare the performance of the developed adaptive acquisition framework with prior non-uniform ADC architectures. The proposed AIQ exhibits power dissipation of 0.32uW for 1-bit resolution, 1uW for 2-bit resolution, 2.33uW for 3-bit resolution, 5.02uW for 4-bit resolution, 10.37uW for 5-bit resolution, 21.08uW for 6-bit resolution, 42.48uW for 7-bit resolution, and 85.3uW for 8-bit resolution. Furthermore, our results indicate that the energy consumption per sample for 1-bit, 2-bit, 3-bit, 4-bit, 5-bit, 6-bit, 7-bit, and 8-bit quantization resolutions are 16.68fJ, 51.79fJ, 120.46fJ, 258.54fJ, 533.98fJ, 1.09pJ, 2.19pJ, and 4.39pJ, respectively.

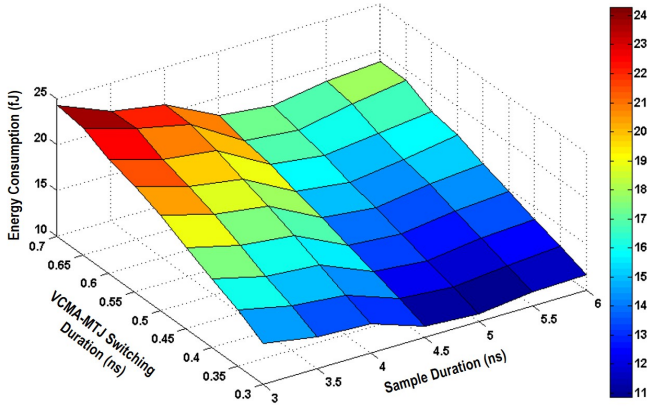
Since our proposed design benefits from intermittent operation, which enables the proposed AIQ to turn off parts of the circuit that are not being utilized during the sampling process and turn them on whenever appropriate, its dynamic power dissipation is averaged from 1-bit to 8-bit resolutions

TABLE II: Comparison with prior ADC designs utilizing Non-Uniform Sampling

	Uniform Digital Output	Process (SupplyVoltage)	Adaptive		Power (Average Power)	Maximum Effective Bandwidth	Energy per Sample
			SR	QR (#Bits)			
Bellasi, et al. [1]	No	28nm (1.0V)	Yes ✓	No (4-bit)	7.5mW	2.4 GHz	2.9 pJ
Varshney, et al. [2]	No	45nm (1.2V)	Yes ✓	Yes ✓ (4-6 bit)	80μW-1.15mW (442μW)	120 MHz	3.68 pJ
Wu, et al. [3]	Yes ✓	65nm (1.0V)	Yes ✓	No (4-bit)	30mW	20 MHz	5 pJ
Naraghi, et al. [4]	No	90nm (1.0V)	Yes ✓	No (9-bit)	14μW	300 KHz	98 fJ
Kurchuk, et al. [5]	Yes ✓	65nm (1.2V)	Yes ✓	Yes ✓ (1-3 bit)	1.1mW-10mW (6.2mW)	2.4 GHz	36 fJ
AIQ (herein)	Yes ✓	22nm (1.0V)	Yes ✓	Yes ✓ (1-8 bit)	0.319μW-85.302μW (20.98μW)	500 MHz	1 pJ



(a)



(b)

Fig. 13: (a) The sample operation error rate trade-off with sample duration and VCMA-MTJ switching duration, and (b) The energy consumption trade-off with sample duration and VCMA-MTJ switching duration.

for a single sample. It should be noted that the amount of energy required for our proposed framework depends on the SR and QR values adapted for each frame. Hence, we report the power consumed averaged for different number of bits in a frame. According to our simulation results, the proposed acquisition framework incurs only 20.98μW power dissipation on average, while providing uniform digital output of 1 to 8 bits. Furthermore, our results indicate that our AIQ architecture on average consumes $\sim$ 1pJ energy per sample.

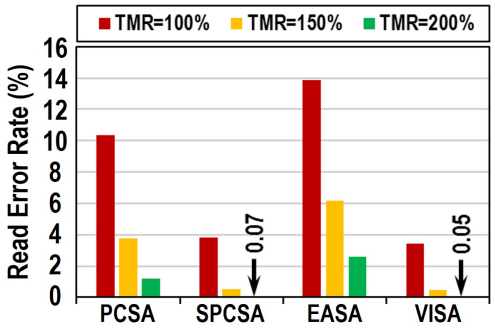


Fig. 14: The read operation error rate trade-off with different TMR values for PCSA, EASA, SPCSA, and VISA.

As it can be observed in Table II, our proposed AIQ design provides 421μW and 6.18mW power savings on average compared to other adaptive rate and resolution ADC designs proposed in [2] and [5], respectively, while offering a wider range of quantization resolution up to 8 bits. Additionally, our proposed AIQ design consumes $\sim$ 1.34pJ less energy per sample on average compared to other state-of-the-art ADC designs proposed in [1–5]. Moreover, despite utilizing an adaptive clock for sampling operation, our proposed AIQ design utilizing VCMA-MTJ spin-based devices achieves a performance comparable with other state of the art CMOS-based architecture as shown in Table II in terms of average power dissipation and energy consumption per sample, while providing adaptive SR and QR.

Moreover, since the MTJ devices are considered as non-volatile memory cells, there is no need for an external FLASH memory or latch to store the data after each sampling operations. The sampled data will remain in the MTJ devices even if the power failure occurs. As a result, an extreme area reduction is achieved. For example, in the 8-bit resolution ADC, 256 comparators are used, and each comparator is connected to a latch for storing the sampled value. However, by utilizing MTJ devices, 256 latches can be eliminated from the circuit, resulting in a significant area reduction. Furthermore, since the MTJ devices can be fabricated on top of the baseline CMOS process, they need not occupy extra area in lateral space, which further advances an area efficient design.

VI. Conclusion

To advance energy-sparing sampling methods , the contributions of the developed cross-layer design can be summarized as follows: (1) a novel framework for efficient and intelligent sensing through the integration of resource allocation, quantized compressive sensing, and configurable spin-based devices are introduced using a multilayered approach, (2) the utility of VCMA-MTJ devices within the proposed AIQ architecture are demonstrated to realize rapid and more energy-efficient sampling and signal processing while achieving reduced area footprint compared to conventional CMOS designs is demonstrated, (3) the energy consumption of VCMA-MTJ is formulated and the energy equation that was derived was then utilized for SR/QR optimization, (4) SR and QR trade-off under resource constraints are studied and an energy-aware adaptive SR/QR optimization framework to tune the sampling rate and quantization resolution is demonstrated, and (5) the adaptive SR/QR controller is integrated with the proposed AIQ for energy-efficient signal acquisition. Finally, the novel sampling and reconstruction algorithms, which have been developed in the context of adaptive quantized CS, open the door to broader applications beyond those addressed in this paper.

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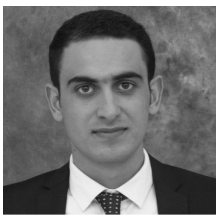
Soheil Salehi (S'15) is currently working towards Ph.D. degree in Computer Engineering at University of Central Florida (UCF). He received his M.S. from UCF in 2016. His research interests include Reconfigurable and Adaptive Computer Architectures, Spintronic-Based Computing Architectures, Low Power and Reliability-Aware VLSI Circuits and Systems, and Deep Submicron Technology Challenges.

Mahdi Boloursaz Mashhadi (S'13) received a dual major B.S. degree (with honors) in communications and industrial engineering in 2011 and the M.S. degree in communications in 2013 from Sharif University of Technology (SUT), Tehran, Iran, where he is pursuing his Ph.D. degree. He is currently a visiting researcher at the ECE department at the University of Central Florida (UCF). He has been a lecturer with the Electrical Engineering Department at SUT during 2014-2016. His research interests encompass sparse signal processing and applications, design and implementation of signal processing circuits and systems, and image, speech, and multimedia processing. Mr. Boloursazs awards and honors include a best paper award at the EWDTS 2012 conference, and two IEEE student travel grants.



Alireza Zaeemzadeh (S'11) received the B.S. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 2014. He is currently working toward Ph.D. degree in electrical engineering at the University of Central Florida. His current research interests lie in the areas of statistical signal processing and Bayesian data analysis. Mr. Zaeemzadeh's awards and honors include University of Central Florida Multidisciplinary Doctoral Fellowship and Graduate Dean's Fellowship.

Nazanin Rahnavard (S'97-M'10) received her Ph.D. in the School of Electrical and Computer Engineering at the Georgia Institute of Technology, Atlanta, in 2007. She is currently an Associate Professor in the Department of Electrical and Computer Engineering at the University of Central Florida, Orlando, Florida. Dr. Rahnavard is the recipient of NSF CAREER award in 2011. She has interest and expertise in a variety of research topics in the communications, networking, and signal processing areas. She serves on the editorial board of the Elsevier Journal on Computer Networks (COMNET) and on the Technical Program Committee of several prestigious international conferences.

Ronald F. DeMara (S'87-M'93-SM'05) has been a full-time faculty member at the University of Central Florida since 1993. His interests are in computer architecture, reconfigurable logic, and emerging devices, on which he has published approximately 225 articles and holds one patent. He is a Senior Member of IEEE and has served on the Editorial Boards of IEEE Transactions on VLSI Systems, IEEE Transactions on Computers, and as Associate Guest Editor of ACM Transactions on Embedded Computing Systems. He has been Keynote Speaker at IEEE RAW and IEEE ReConFig conferences, and Guest Editor of IEEE Transactions on Emerging Topics in Computing joint with IEEE Transactions on Computers 2017 Special Section on Innovation in Reconfigurable Fabrics. He received the Joseph M. Bidenbach Outstanding Engineering Educator Award from IEEE in 2008.